Hard disk drive specifications

Travelstar 32GH, 30GT & 20GN

2.5 inch ATA/IDE hard disk drive

Models: DJSA-232 DJSA-210
DJSA-230 DJSA-205
DJSA-220

Revision 4.0

7 December 2001

S07N-3499-05

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1.0 Introduction

This document describes the specifications of the following IBM 2.5 inch, ATA/IDE interface hard disk drives:

- DJSA-232 (32 GB)
- DJSA-230 (30 GB)
- DJSA-220 (20 GB)
- DJSA-210 (10 GB)
- DJSA-205 (5 GB)

Part 1 of this document defines the hardware functional specification. For details about the interface specification refer to Part 2 of this document.

Note: These specifications are subject to change without notice.

1.1 Abbreviations

Abbreviation	*Meaning*
32 KB	32 x 1024 bytes
64 KB	64 x 1024 bytes
"	inch
A	amp
AC	alternating current
AT	Advanced Technology
ATA	Advanced Technology Attachment
Bels	unit of sound power
BIOS	Basic Input/Output System
°C	degrees Celsius
°C/Hour	degrees Celsius per hour
CSA	Canadian Standards Association
C-UL	Canadian-Underwriters Laboratory
Cyl	cylinder
DC	direct current
DFT	Drive Fitness Test
DMA	Direct Memory Access
ECC	error correction code
EEC	European Economic Community
EMC	electromagnetic compatibility
ERP	Error Recovery Procedure
ESD	electrostatic discharge
FCC	Federal Communications Commission
FRU	field replacement unit
G	gravity, a unit of force
Gb	1 000 000 000 bits
GB	1 000 000 000 bytes
Gb/sq.in.	1 000 000 000 bits per square inch
G^2/Hz	$(32 \text{ ft/sec})^2$ per Hertz
GND	ground
h	hexadecimal
HDA	head disk assembly

HDD	hard disk drive
Hz	hertz
I	Input
ILS	integrated lead suspension
imped	impedance
I/O	Input/Output
ISO	International Standards Organization
KB	1,000 bytes
Mbits/sec	1,000,000 bits per second
Kbpi	1,000 Bit Per Inch
kgf-cm	kilogram (force)-centimeter
KHz	kilohertz
LBA	logical block addressing
Lw	unit of A-weighted sound power
m	meter
max. or Max.	maximum
MB	1,000,000 bytes
Mbps	1,000,000 Bit per second
Mb/sec	1,000,000 Bit per second
MB/sec	1,000,000 bytes per second
Mb/sq.in.	1,000 ,00 bits per square inch
MHz	megahertz
MLC	Machine Level Control
mm	millimeter
ms	millisecond
us	microsecond
No. or #	number
oct/min	oscillations per minute
O	Output
OD	Open Drain
PIO	Programmed Input/Output
POH	power on hours
Pop.	population
P/N	part number
p-p	peak-to-peak
PSD	power spectral density
RES	radiated electromagnetic susceptiblity
RFI	radio frequency interference
RH	relative humidity
% RH	per cent relative humidity
RMS	root mean square
RPM	revolutions per minute
RST	reset
R/W	read/write
sec	second
Sect/Trk	sectors per track
SELV	secondary low voltage
S.M.A.R.T	Self-monitoring, analysis, and reporting technology
TPI	tracks per inch
Trk.	track
TTL	transistor-transistor logic
UL	Underwriters Laboratory
V	volt
VDE	Verband Deutscher Electrotechniker

W	watt
3-state	transistor-transistor tristate logic

1.2 References

- ATA/ATAPI-5 (T13/1321D Revision D)

1.3 General caution

- Do not apply force to the top cover (See Figure 1 on page 4).
- Do not cover the breathing hole on the top cover (See Figure 1 on page 4).
- Do not touch the interface connector pins or the surface of the printed circuit board.
- The drive can be damaged by shock or ESD (Electric Static Discharge). Any damages incurred to the drive after removing it from the shipping package and the ESD protective bag are the responsibility of the user.

1.4 Drive handling precautions

Do not press on the drive cover during handling.

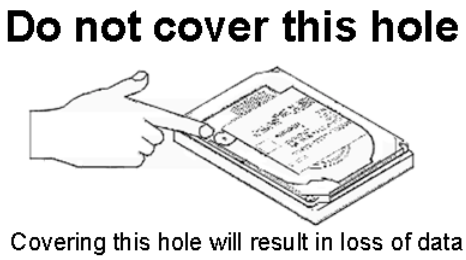

Figure 1. Drive handling precautions

2.0 General features

- Height MCC Compliance
  - (DJSA-232/230) 2.5 inch, 12.5±0.2 mm
  - (DJSA-220/210/205) 2.5 inch, 9.5±0.2 mm
- Drive formatted capacity by model number
  - (DJSA-232) 32 GB
  - (DJSA-230) 30 GB
  - (DJSA-220) 20 GB
  - (DJSA-210) 10 GB
  - (DJSA-205) 5 GB
- 512 bytes/sector
- AT Interface (Enhanced IDE) conforming to ATA-5
- Integrated controller
- No ID recording format
- Coding: 32/34
- Multizone recording
- Enhanced ECC on-the-fly
  - 40 bytes 3 way Interleaved Reed Solomon Code
  - 5 bytes per interleave on-the-fly correction
- Segmented Buffer with write cache
  - 2 MB - Upper 174KB is used for firmware (DJSA-232/230/220)
  - 512 KB - Upper 128KB is used for firmware (DJSA-210/205)
- Fast data transfer rate (up to 66.6 MB/sec)
- Media data transfer rate
  - 203 (outer zone) - 109 (inner zone) Mb/sec (DJSA-230/220/210/205)
  - 223 (outer zone) - 120 (inner zone) Mb/sec (DJSA-232)
- Average seek time 12 ms for read
- Closed-loop actuator servo (Embedded Sector Servo)
- Rotary voice coil motor actuator
- Load/Unload mechanism
- Mechanical latch
- Adaptive power save control
  - 0.65 W at idle state (DJSA-220/210/205)
  - 0.85 W at idle state (DJSA-230)
  - 0.9 W at idle state (DJSA-232)

- Power on to ready
  - 5.0 sec (DJSA-232)
  - 3.3 sec (DJSA-230)
  - 3.0 sec (DJSA-220/210/205)
- Nonoperating Shock
  - 700 G 1ms (DJSA-232/230)
  - 800 G 1 ms (DJSA-220/210/205)
- Operating Shock
  - 150 G 2 ms (DJSA-232)
  - 175 G 2 ms (DJSA-230/220/210/205)
- Address Offset Feature to support DFT implementation

Note: Mounting screw position is

- *incompatible with DBOA,DMCA, DCRA, DSOA, DPRA models.*
- *compatible with DTNA, DLGA, DDLA, DTCA, DPLA, DYKA, DYLA, DADA, DKLA, DBCA, DCXA, DCYA, DARA models.*

Part 1. Functional specification

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3.0 Fixed disk subsystem description

3.1 Control Electronics

The control electronics works with the following functions.

- AT Interface Protocol
- Embedded Sector Servo
- No-ID formatting
- Multizone recording
- Code: 32/34
- ECC on-the-fly
- Enhanced Adaptive Battery Life Extender

3.2 Head disk assembly data

The following technologies are used in each DJSA-XXX model.

- Pico Slider
- Smooth glass disk
- GMR head
- Integrated lead suspension (ILS)
- Load/unload mechanism
- Mechanical latch

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4.0 Fixed disk characteristics

4.1 Default logical drive parameters

The following table lists the default logical drive parameters by drive model number.

Model	Capacity (GB)	Word 1 (Cyl)	Word 3 (Head)	Word 6 (Sect/Trk)	Word 60–61 (LBA)	Customer Usable Data Bytes
DJSA-232	32	16,383	16	63	3B9C460h	32,003,112,960
DJSA-230	30	16,383	16	63	37E3E40h	30,005,821,440
DJSA-220	20	16,383	16	63	2542980h	20,003,880,960
DJSA-210	10	16,383	16	63	12BB230h	10,056,130,560
DJSA-205	5	10,336	15	63	950A60h	5,000,970,240

Figure 2. Default logical drive parameters

4.2 Formatted capacity by model number

Description	DJSA-232	DJSA-230	DJSA-220	DJSA-210	DJSA-205
Physical Layout					
Bytes per Sector	512	512	512	512	512
Sectors per Track	256-469	293–560	293–560	293–560	293–560
Number of Heads	8	6	4	2	1
Number of Disks	4	3	2	1	1
Logical Layout					
Number of Heads	16	16	16	16	15
Number of Sectors/ Track	63	63	63	63	63
Number of Cylinders	62,010	58,140	38,760	19,485	10,336
Number of Sectors	62,506,080	58,605,120	39,070,080	19,640,880	9,767,520
Total Logical Data Bytes	32,003,112,960	30,005,821,440	20,003,880,960	10,056,130,560	5,000,970,240

Figure 3. Formatted capacity by model number.

4.3 Data sheet

	DJSA-232	DJSA-230/220/210/205
Rotational Speed (RPM)	5400	4200
Data transfer rates (buffer to/from media)	120-223 Mbps	109-203 Mbps
Interface transfer rate (MB/sec) ULTRA DMA 66	66.6 MB/sec	66.6 MB/sec
Recording density (Kbpi) (Max.)	399	451
Track density (Ktpi)	36	38
Areal density (Gb/sq.in.)(Max.)	14.4	17.1
Number of zones	16	16

Figure 4. Data sheet

4.4 Cylinder allocation by model number

	DJSA-232		DJSA-230/220/210/205	
Zone	**Cylinder**	**No. of Sectors/Trk**	**Cylinder**	**No. of Sectors/Trk**
0	0–255	469	0–767	560
1	256–1023	460	768–1535	560
2	1024–3071	448	1536–3583	533
3	3072–4095	426	3584–4863	520
4	4096–5631	416	4864–5887	506
5	5632–7167	400	5888–7423	480
6	7168–8959	384	7424–8959	480
7	8960–10751	362	8960–10751	453
8	10752–12287	352	10752–12031	440
9	12288–13567	352	12032–13567	420
10	13568–15615	336	13568–15615	400
11	15616–17407	320	15616–16895	380
12	17408–18943	298	16896–18687	360
13	18944–19967	288	18688–19967	340
14	19968–21247	272	19968–22015	320
15	21248–21503	256	22016–22783	293

Figure 5. Cylinder allocation by model number

4.5 Performance characteristics

File performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
  - Seek Time
  - Latency
- Data Transfer Speed
- Buffering Operation (Look ahead/Write Cache)

Note: All the above parameters contribute to file performance. There are other parameters which contribute to the performance of the actual system. This specification defines the essential file characteristics. This specification does not include the system throughput as this is dependent upon the system and the application.

The following table gives a typical value for each parameter. The detail descriptions are found in section 5.0.

Function	Typical DJSA-232	Typical DJSA-230	Typical DJSA-220/210/205
Average Random Seek Time For Read (ms)	12	12	12
Average Random Seek Time For Write (ms)	13	13	13
Rotational Speed (RPM)	5400	4200	4200
Power-on-to-ready (sec)	5.0	3.3	3.0
Command overhead (ms)	1.0	1.0	1.0
Disk-buffer data transfer (Mb/s)	120-223	109-203	109–203
Buffer-host data transfer (MB/s) (PIO Mode-4) (Ultra DMA Mode-4)	16.6 66.6	16.6 66.6	16.6 66.6

Figure 6. Performance characteristics

4.5.1 Command overhead

Command overhead time is defined as the interval from the time that a drive receives a command to the time that the actuator starts its motion.

4.5.2 Mechanical positioning

4.5.2.1 Average seek time (including settling)

Command Type	Typical (ms)	Max. (ms)
Read	12	14
Write	13	15

Figure 7. Mechanical positioning performance

Typical and Max. are defined throughout the performance specification as follows:

Typical Average of the drive population tested at nominal environmental and voltage conditions.

Max. Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See section 6.1 on Environment and section 6.2 on DC power requirements.)

The seek time is measured from the start of motion of the actuator to the start of a reliable read or write operation. A reliable read or write operation implies that error correction/recovery is not employed to correct arrival problems. The Average Seek Time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\text{max.}} (\text{max.} + 1 - n)(Tn_{in} + Tn_{out})}{(\text{max.} + 1)(Tn_{in} + Tn_{out})}$$

Where: max. = maximum seek length

n = seek length (1-to-max.)

Tn_{in} = inward measured seek time for an n-track seek

Tn_{out} = outward measured seek time for an n-track seek

4.5.2.2 Full stroke seek

Command Type	Typical (ms)	Max. (ms)
Read	23.0	30
Write	24.0	31

Figure 8. Full stroke seek time

Full stroke seek time in milliseconds is the average time of 1000 full stroke seeks.

4.5.2.3 Single track seek time (without command overhead, including settling)

Command Type	Typical (ms)	Maximum (ms)
Read	2.5	4.0
Write	3.0	4.5

Figure 9. Single track seek time

Single track seek is measured as the average of one (1) single track seek from every track in both directions (inward and outward).

4.5.2.4 Average latency

Model	Rotational Speed (RPM)	Time/1 revolution (ms)	Average Latency (ms)
DJSA-232	5400	11.1	5.5
DJSA-230/220/210/205	4200	14.3	7.1

Figure 10. Latency time

4.5.2.5 Drive ready time

Condition	Model	Typical (sec)	Max. (sec)
Power On To Ready	DJSA-232	5.0	9.5
Power On To Ready	DJSA-230	3.3	9.5
Power On To Ready	DJSA-220/210/205	3.0	9.5

Figure 11. Drive ready time

Ready The condition in which the drive is able to perform a media access command (for example—read, write) immediately.

Power On To Ready This includes the time required for the internal self diagnostics.

4.5.3 Operating modes

Operating mode	*Description*
Spin-Up:	Start up time period from spindle stop or power down.
Seek:	Seek operation mode
Write:	Write operation mode
Read:	Read operation mode
Performance:	The device is capable of responding immediately to idle media access requests. All electronic components remain powered and the full frequency servo remains operational.
Active idle:	The device is capable of responding immediately to media access requests. Some circuitry—including servo system and R/W electronics—is in power saving mode. The head is parked near the mid-diameter the disk without servoing. A device in Active idle mode may take longer to complete the execution of a command because it must activate that circuitry.
Low power idle:	The head is unloaded onto the ramp position. The spindle motor is rotating at full speed.
Standby:	The device interface is capable of accepting commands. The spindle motor is stopped. All circuitry but the host interface is in power saving mode. The execution of commands is delayed until the spindle becomes ready.
Sleep:	The device requires a soft reset or a hard reset to be activated. All electronics, including spindle motor and host interface, are shut off.

Figure 12. Operating mode

4.5.3.1 Mode transition time

Model	From	To	Transition Time (typ)	Transition Time (max.)
DJSA-232	Standby	Idle	4.5	9.5
DJSA-230/220	Standby	Idle	2.0	9.5
DJSA-210/205	Standby	Idle	1.8	9.5

Figure 13. Drive ready time

4.5.3.2 Operating mode at power on

The device goes into Idle mode after power on or hard reset as an initial state. Initial state may be changed to Standby mode using pin C on the interface connector. Refer to section 7.10 on page 57, "Drive address setting", for details.

4.5.3.3 Adaptive power save control

The transient timing from Performance Idle mode to Active Idle mode, from Active Idle mode to Low Power Idle mode, and from Low Power Idle mode to Standby mode is controlled adaptively according to the access pattern of the host system in order to reduce the average power dissipation.

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5.0 Data integrity

5.1 Data loss on power off

- Data loss will not be caused by a power off during any operation but the write operation.
- A power off during a write operation causes the loss of any received or resident data that has not been written onto the disk media.
- A power off during a write operation might make a maximum of one sector of data unreadable. This state can be recovered by a rewrite operation.

5.2 Write Cache

When the write cache is enabled the write command may complete before the actual disk write operation finishes. This means that a power off, even after the write command completion, could cause the loss of data that the drive has received but not yet written onto the disk.

In order to prevent this data loss, confirm the completion of the actual write operation prior to the power off by issuing a

- Soft reset
- Hard reset
- Flush Cache command
- Standby command
- Standby Immediate command
- Sleep command

Confirm the command's completion.

5.3 Equipment status

The equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at the power-on time and will be maintained until the following conditions are satisfied:

- The access recalibration/tuning is complete.
- The spindle speed meets the requirements for reliable operation.
- The self-check of the drive is complete.

The appropriate error status is made available to the host system if any of the following conditions occur after the drive has become ready:

- The spindle speed lies outside the requirements for reliable operation.
- The occurrence of a Write Fault condition.

5.4 WRITE safety

The drive ensures that the data is written into the disk media properly. The following conditions are monitored during a write operation. When one of these conditions exceeds the criteria, the write operation is terminated and the automatic retry sequence is invoked.

- Head off track
- External shock
- Low supply voltage
- Spindle speed out of tolerance
- Head open/short

5.5 Data buffer test

The data buffer is tested at power on reset and when a drive self-test is requested by the host. The test consists of a write/read '00'x and 'ff'x pattern on all buffers.

5.6 Error recovery

Errors occurring on the drive are handled by the error recovery procedure.

Errors that are uncorrectable after application of the error recovery procedure are reported to the host system as nonrecoverable errors.

5.7 Automatic reallocation

The sectors that show some errors may be reallocated automatically when specific conditions are met. The drive does not report any auto reallocation to the host system. The conditions for auto reallocation are described below.

5.7.1 Nonrecovered write errors

When a write operation cannot be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation has failed.

5.7.2 Nonrecoverable read error

When a read operation fails after ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the required criteria, this sector is reallocated.

5.7.3 Recovered read errors

When a read operation for a sector fails and is recovered at the specific ERP step, the sector is reallocated automatically. A media verification sequence may be run prior to the reallocation according to the predefined conditions.

5.8 ECC

The 40 byte three interleaved ECC processor provides user data verification and correction capability. The first 4 bytes of ECC are check bytes for user data and the other 36 bytes are Read Solomon ECC. Each interleave has 12 bytes for ECC. Hardware logic corrects up to 15 bytes (5 bytes for each interleave) errors on-the-fly.

Following are some examples of error cases. An "O" means that the byte contains no error. An "X" means that at least one bit of the byte is bad.

On The Fly correctable

Byte #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	Error byte # for each interleave		
Interleave	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
Error pattern	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	O	O	O	5	5	5
Error pattern	X	X	X	X	X	X	X	X	X	O	O	O	X	X	X	X	X	X	5	5	5

Uncorrectable

Byte #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	Error byte # for each interleave		
Interleave	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
Error pattern	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	O	O	6	5	5
Error pattern	X	O	O	X	O	O	X	O	O	X	O	O	X	O	O	X	O	O	6	0	0

Figure 14. Examples of error cases.

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6.0 Specification

6.1 Environment

6.1.1 Temperature and humidity

Operating conditions	
Temperature	5 to 55°C (See Note)
Relative humidity	8 to 90% noncondensing
Maximum wet bulb temperature	29.4°C noncondensing
Maximum temperature gradient	20°C/hour
Altitude	–300 to 3048 m (10,000 ft)
Nonoperating conditions	
Temperature	–40 to 65°C
Relative humidity	5 to 95% noncondensing
Maximum wet bulb temperature	40°C noncondensing
Maximum temperature gradient	20°C/hour
Altitude	–300 to 12,192 m (40,000 ft)
Note: The system is responsible for providing sufficient air movement to maintain surface temperatures below 60°C at the center of top cover and below 63°C at the center of the drive circuit board assembly.	

Figure 15. Environmental condition

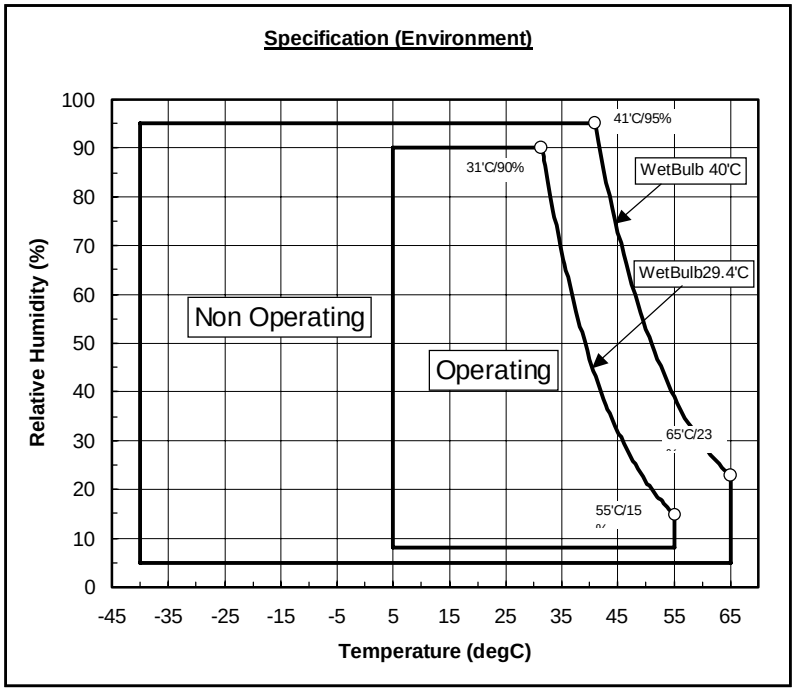

Figure 16. Limits of temperature and humidity

6.1.1.1 Corrosion test

The hard disk drive must be functional and show no signs of corrosion after being exposed to a temperature humidity stress of 50°C/90%RH (relative humidity) for one week followed by a temperature humidity drop to 25°C/40%RH in 2 hours.

6.1.2 Magnetic fields

The disk drive will withstand radiation and conductive noise within the limits shown below.

6.1.2.1 Radiation noise

The disk drive shall work without degradation of the soft error rate under the following magnetic flux density limits at the enclosure surface.

Frequency (KHz)	Limits (Gauss RMS)
0–60	5
61–100	2.5
101–200	1
201–400	0.5

Figure 17. Magnetic flux density limits

6.1.2.2 Conductive noise

The disk drive shall work without soft error degradation in the frequency range from DC to 20 Mhz injected through any two of the mounting screw holes of the hard disk drive (HDD) when an AC current of up to 45 mA (p-p) is applied through a series 50 ohm resistor connected to any two mounting screw holes.

6.2 DC power requirements

Connection to the product should be made in isolated secondary circuits (SELV). The voltage specifications are applied at the power connector of the drive.

Item	Requirements	Notes
Nominal Supply	+5 Volt dc	
Power Supply Ripple (0–20 MHz)	100 mV p-p max.	*1
Tolerance	±5%	*2
Supply rise time	7–100 ms	
Supply Current (+5.00 V dc case)	Population Mean (nominal condition)	

Watts (RMS Typical)	DJSA-232	DJSA-230	DJSA-220/210/205	Notes
Performance Idle average	2.0	1.85	1.85	*3
Active Idle average	1.3	0.95	0.85	
Low Power Idle average	0.9	0.65	0.65	
Read average	2.5	2.1	2.0	*4
Write average	2.7	2.2	2.1	
Seek average	2.6	2.3	2.3	*5
Standby	0.25	0.25	0.25	
Sleep	0.1	0.1	0.1	
Startup (maximum peak)	5.0	4.7	4.7	*6
Average from power on to ready	3.8	3.3	3.3	

Notes:

**1. The maximum fixed disk ripple is measured at the 5 volt input of the HDD.*

**2. The disk drive shall not incur damage for an over voltage condition of +25% (maximum duration of 20 ms) on the 5 volt nominal supply.*

**3. The idle current is specified at an inner track.*

**4. The read/write current is specified based on three operations of 63 sector read/write per 100 ms.*

**5. The seek average current is specified based on three operations per 100 ms.*

**6. The worst case operating current includes motor surge.*

Figure 18. DC Power requirements

6.2.1 Energy consumption efficiency

Model	Energy consumption efficiency (Watt/Capacity(GB))
DJSA-232/230/220	0.03
DJSA-210/205	0.07

Figure 19. Energy consumption efficiency

Note: Energy consumption efficiency is calculated as Power Consumption of Low Power Idle Watt/ Capacity (GB).

6.3 Startup current

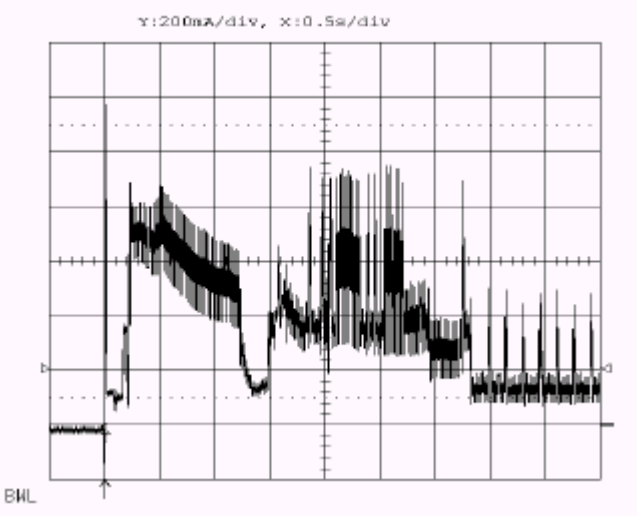

Figure 20. Typical current wave form at start up of DJSA-220/210/205

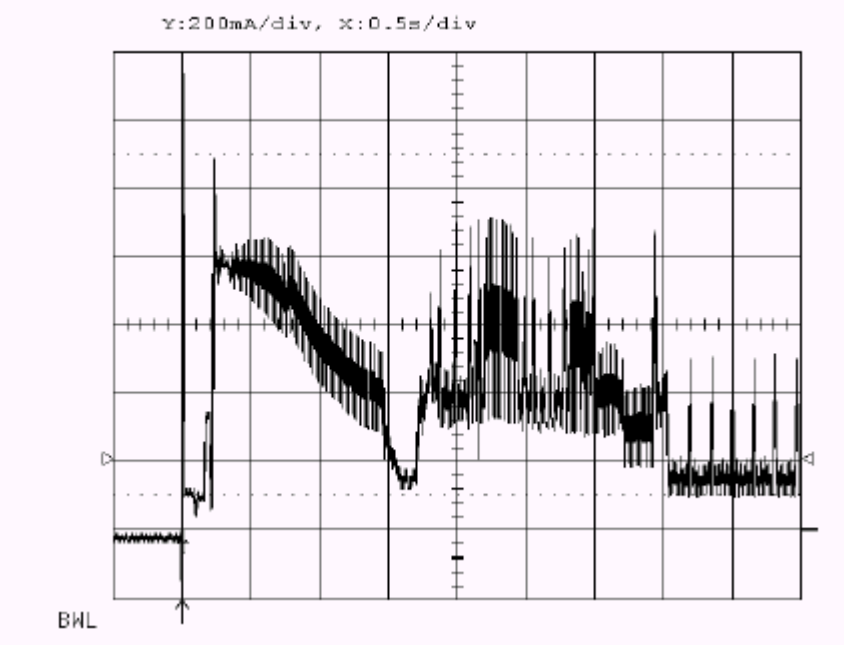

Figure 21. Typical current wave form at start up of DJSA-230

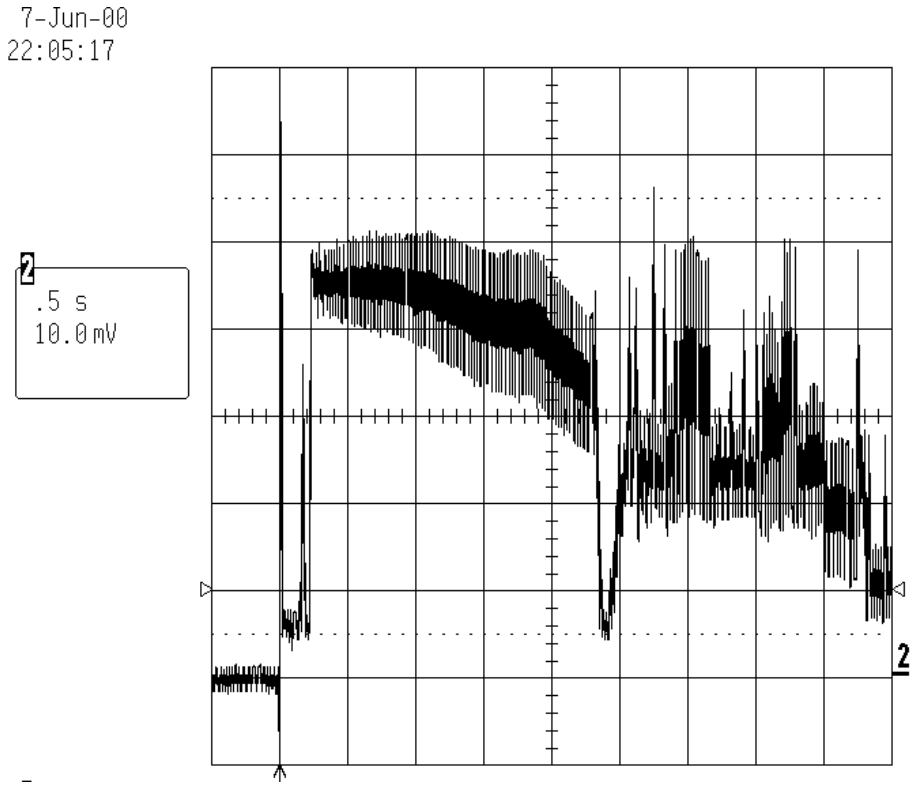

Figure 22. Typical current wave form at start up of DJSA-232

6.4 Reliability

6.4.1 Data reliability

- Probability of not recovering data is 1 in 10^{13} bits read.
- ECC implementation.

  On-the-fly correction—performed as a part of read channel function—recovers up to 15 symbols of error in 1 sector (1 symbol is 8 bits).

6.4.2 Failure prediction (S.M.A.R.T.)

DJSA-XXX supports Self-monitoring, analysis and reporting technology (S.M.A.R.T.) function. The details are described in 11.7, "S.M.A.R.T. Function," on page 80 and 13.32, "S.M.A.R.T. Function Set (B0h)," on 159.

6.4.3 Cable noise interference

To avoid any degradation of performance throughput or error when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.4.4 Service life and usage condition

The drive is designed to be used under the following conditions:

- The drive should be operated within specifications of shock, vibration, temperature, humidity, altitude, and magnetic field.
- The drive should be protected from ESD.
- The breathing hole in the top cover of the drive should not be covered.
- Force should not be applied to the cover of the drive.
- The specified power requirements of the drive should be satisfied.
- The drive frame should be grounded electrically to the system through four screws.
- The drive should be mounted with the recommended screw depth and torque.
- The interface physical and electrical requirements of the drive should satisfy ATA-5.
- The power-off sequence of the drive should comply with the 6.4.6.2,"Required power-off sequence."

Service life of DJSA-2xx is approximately 5 years or 20,000 power on hours, whichever comes first under the following assumptions.

- Less than 333 power on hours per month.
- Seeking/Writing/Reading operation is less than 20% of power on hours.

This does not represent any warranty or warranty period. Applicable warranty and warranty period are covered by the purchase agreement.

6.4.5 Preventive maintenance

None.

6.4.6 Load/unload

The product supports a minimum of 300,000 normal load/unloads.

Load/unload is a functional mechanism of the hard disk drive. It is controlled by the drive micro code. Specifically, unloading of the heads is invoked by the following commands:

- Hard reset
- Soft reset
- Standby
- Standby immediate
- Sleep

Load/unload is also invoked as one of the idle modes of the drive.

The specified start/stop life of the product assumes that load/unload is operated normally, not in emergency mode.

6.4.6.1 Emergency unload

When hard disk drive power is interrupted while the heads are still loaded the micro code cannot operate and the normal 5 volt power is unavailable to unload the heads. In this case, normal unload is not

possible. The heads are unloaded by routing the back EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case and the unload process is inherently less controllable without a normal seek current profile.

Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

DJSA-XXX supports a minimum of 20,000 emergency unloads.

6.4.6.2 Required Power-Off Sequence

The required BIOS sequence for removing power from DJSA-XXX is as follows:

- Step 1: Issue one of the following commands.
  - Soft Reset
  - Standby
  - Standby immediate
  - Sleep

    Note: Do not use the Flush Cache command for the power off sequence because this command does not invoke Unload.
- Step 2: Wait until the Command Complete status is returned.

  In a typical case 350 ms are required for the command to finish completion; however, the BIOS time out value needs to be 30 seconds considering error recovery time. Refer to section 14.0, "Time-out values," on page 187.
- Step 3: Terminate power to HDD.

This power-down sequence should be followed for entry into any system power-down state, system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios, such as battery removal during operation.

6.4.6.3 Power switch design considerations

In systems that use DJSA-XXX, consideration should be given to the design of the system power switch.

IBM recommends that the switch operate under control of the BIOS, as opposed to being hard-wired. The same recommendation is made for cover-close switches. When a hard-wired switch is turned off, emergency unload occurs, as well as the problems cited in section 5.1, "Data loss by power off" on page 19 and section 5.2, “Write Cache” on page 19.

6.4.6.4 Test considerations

Start/stop testing is classically performed to verify head/disk durability. In the case of DJSA-XXX the heads do not land on the disk, so this type of test should be viewed as a test of the load/unload function.

Start/Stop testing should be done by commands through the interface, not by power cycling the drive. Simple power cycling of DJSA-XXX invokes the emergency unload mechanism and subjects the HDD to nontypical mechanical stress.

Power cycling testing may be required to test the boot-up function of the system. In this case IBM recommends that the power-off portion of the cycle contain the sequence specified in section 6.4.6.2, "Required Power-Off Sequence” on page 30. Again, if this is not done, the emergency unload function is invoked and nontypical stress results.

6.5 Mechanical specifications

6.5.1 Physical dimensions and weight

The following figure lists the dimensions for the 2.5 inch hard disk drive form factor.

Model	Height (mm)	Width (mm)	Length (mm)	Weight (gram)
DJSA-232	12.5±0.2	69.85±0.25	100.2±0.25	155 Max.
DJSA-230	12.5±0.2	69.85±0.25	100.2±0.25	135 Max.
DJSA-220/210/205	9.5±0.2	69.85±0.25	100.2±0.25	99 Max.

Figure 23. Physical dimensions and weight

6.5.2 Mounting hole locations

The mounting hole locations and size of the hard disk drive are shown below.

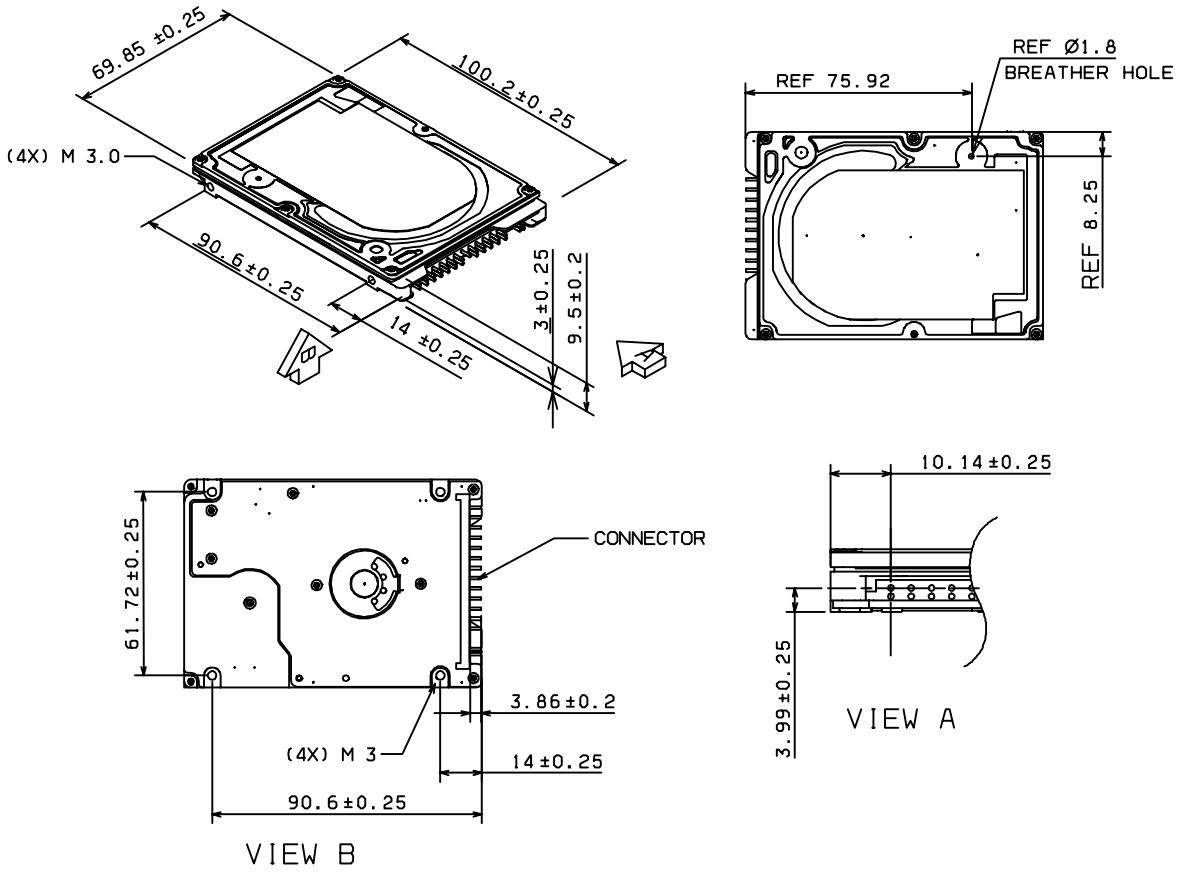

Figure 24. Mounting hole locations of the DJSA-220/210/205

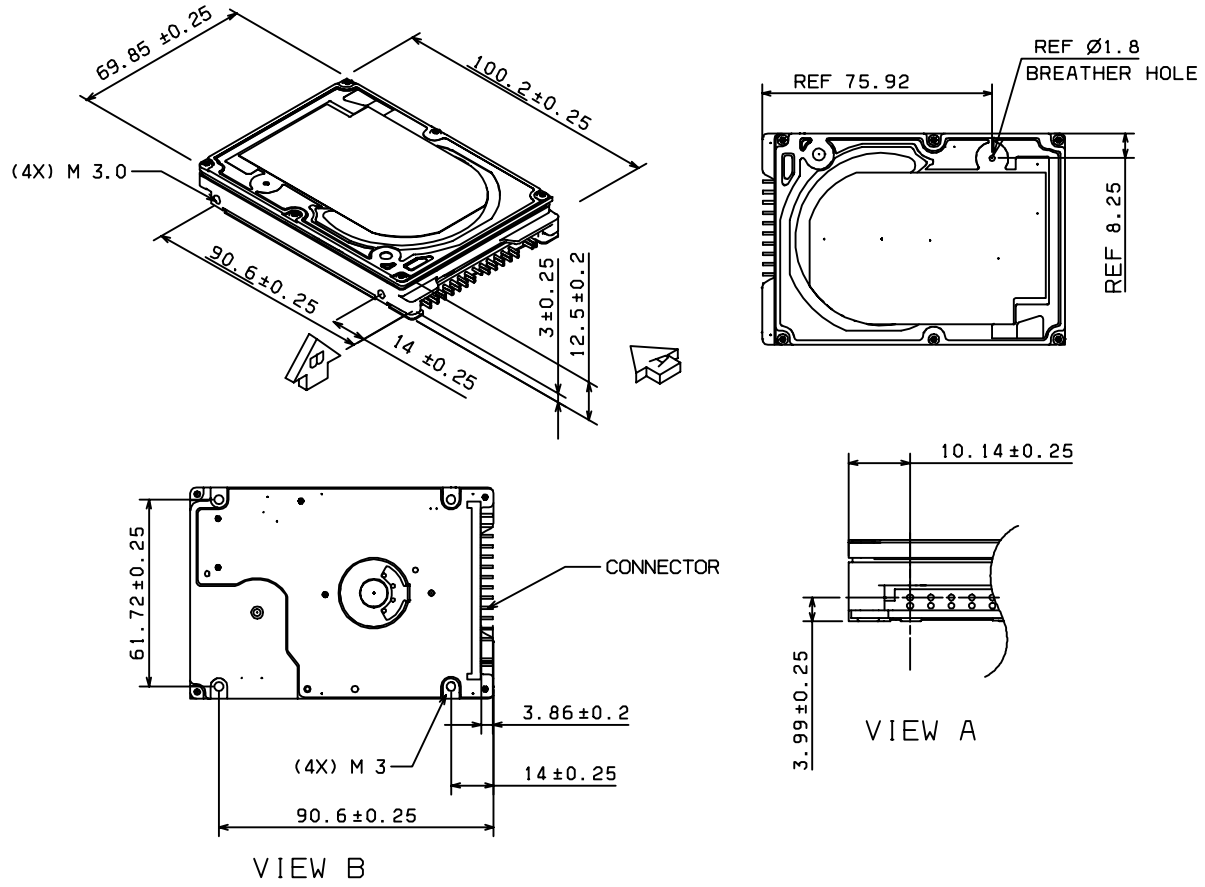

Figure 25. Mounting hole locations of the DJSA-232/230

6.5.3 Connector and jumper description

A jumper is used to designate the drive address as either master or slave. The jumper setting method is described in section 7.10.

Connector specifications are included in Part 2 of this document—Electrical Interface specifications.

6.5.4 Mounting orientation

The drive will operate in all axes (6 directions) and will stay within the specified error rates when tilted ±5 degrees from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The recommended mounting screw torque is 3.0±0.5 kgf-cm.

The recommended mounting screw depth is 3.0±0.3 mm for bottom and 3.5±0.5 mm for horizontal mounting.

The user should use appropriate screws or equivalent mounting hardware to mount the drive securely enough to prevent excessive motion or vibration of the drive at seek operation or spindle rotation.

6.5.5 Load/unload mechanism

The head load/unload mechanism is provided to protect the disk data during shipping, movement, or storage. Upon power down, a head unload mechanism secures the heads at the unload position. See 6.6.4, "Nonoperating shock", on page 36 for additional details.

6.6 Vibration and shock

All vibration and shock measurements in this section are for hard disk drives without mounting attachments for systems. The input level shall be applied to the normal drive mounting points.

Vibration tests and shock tests are to be conducted by mounting the drive to a table using the bottom four mounting holes.

6.6.1 Operating vibration

The disk drive will operate without a hard error while being subjected to the following vibration levels.

6.6.1.1 Random vibration

The test will be 30 minutes of random vibration using the power spectral density (PSD) levels below. The vibration test level is 0.67 G RMS (Root Mean Square).

Random vibration PSD profile Breakpoint	
	DJSA-205/210/220/230/232
Hz	m x 10^n G^2/Hz
5	2.0 x E–5
17	1.1 x E–3
45	1.1 x E–3
48	8.0 x E–3
62	8.0 x E–3
65	1.0 x E–3
150	1.0 x E–3
200	5.0 x E–4
500	5.0 x E–4

Figure 26. Random vibration PSD profile breakpoints (operating)

6.6.1.2 Swept sine vibration

	Swept sine vibration (zero to peak 5 to 500 to 5 Hz sine wave)	**Sweep rate (oct/min)**
DJSA-205/210/220/230	1 G (5-500 Hz)	2.0
DJSA-232	1 G (5-300 Hz) 1 G (300 Hz) - 0.33 G (350 Hz) 0.33 G (350-500 Hz)	2.0

Figure 27. Swept sine vibration

6.6.2 Nonoperating vibration

The disk drive withstands the following vibration levels without any loss or permanent damage.

6.6.2.1 Random vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with the time duration of 15 minutes per axis. The PSD levels for the test simulating the shipping and relocation environment is shown below.

Hz	G^2/Hz
2.5	0
5	0.03
40	0.02
500	0.02

Note: Overall RMS level of vibration is 3.01 G.

Figure 28. Random Vibration PSD Profile Breakpoints (nonoperating)

6.6.2.2 Swept sine vibration

- 5 G (zero-to-peak), 5 to 500 to 10 Hz sine wave
- 0.5 oct/min sweep rate
- 25.4 mm (peak-to-peak) displacement, 5 to 10 to 5 Hz

6.6.3 Operating shock

The hard disk drive meets the following criteria while operating in the conditions described below.

The shock test consists of ten shock inputs in each axis and direction for a total of 60.

There must be a minimum 3 seconds delay between shock pulses.

The disk drive will operate without a hard error while being subjected to the following half-sine shock pulse.

Model	Duration of 2 ms	Duration of 11 ms
DJSA-232	150 G	15 G
DJSA-230/220/210/205	175 G	15 G

Figure 29. Operating shock

The input level shall be applied to the normal disk drive subsystem mounting points used to secure the drive in a normal system.

6.6.4 Nonoperating shock

The drive withstands the following half-sine shock pulse without any data loss or permanent damage.

Model	Duration of 1 ms	Duration of 11 ms
DJSA-232/230	700 G	120 G
DJSA-220/210/205	800 G	120 G

Figure 30. Nonoperating shock

The shocks are applied for each direction of the drive for three mutually perpendicular axes, one axis at a time. Input levels are measured on a base plate where the drive is attached with four screws.

6.7 Acoustics

6.7.1 Sound power level

The criteria of A-weighted sound power level are described below.

Measurements are to be taken in accordance with ISO 7779. The mean of the sample of 40 drives is to be less than the typical value. Each drive is to be less than the maximum value. The drives are to meet this requirement in both board down orientations.

A-weighted Sound Power	Typical (Bels)	Maximum (Bels)
DJSA-232		
Idle	2.5	2.7
Operating	3.5	3.8
DJSA-230		
Idle	2.8	3.4
Operating	3.5	3.8
DJSA-220/210/205		
Idle	2.8	3.4
Operating	3.3	3.6

Figure 31. Weighted sound power

The background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive be located 25±3 mm above from the chamber floor. No sound absorbing material shall be used.

The acoustical characteristics of the disk drive are measured under the following conditions.

Mode definitions

- Idle mode—Power on, disks spinning, track following, unit ready to receive and respond to control line commands.
- Operating mode—Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as shown below.
  - Ns = 0.4/(Tt + T1)

  where:
  - Ns = average seek rate in seeks/s
  - Tt = published seek time from one random track to another without including rotational latency
  - T1= equivalent time, in seconds, for the drive to rotate by half a revolution

6.7.2 Discrete tone penalty

Discrete tone penalties are added to the A-weighted sound power (Lw) with the following formula only when determining compliance.

Lwt(spec) = Lw = 0.1Pt + 0.3 < 4.0 (Bels)

Lw = A-weighted sound power level

Pt = Value of desecrate tone penalty = dLt – 6.0(dBA)

dLt = Tone-to-noise ratio taken in accordance with ISO 7779 at each octave band.

6.8 Identification labels

The following labels are affixed to every disk drive.

- A label is placed on the top of the HDA containing the statement "Made by IBM" or equivalent, Part No., EC No. and FRU No.
- A bar code label placed on the disk drive based on user request. The location on the disk drive is to be designated in the drawing provided by the user.
- Labels containing the vendor's name, disk drive model number, serial number, place of manufacture and UL/CSA logos.
- The presence of labels containing jumper information depends on customers.

6.9 Electromagnetic compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, shall meet the following worldwide electromagnetic compatibility (EMC) requirements:

- United States FCC (Federal Communications Commission) Rules and Regulations (Class B), Part 15.
- RFI Suppression German National Requirements.
- RFI Japan VCCI Requirements of IBM products.
- EU EMC Directive Technical Requirements and Conformity Assessment Procedures.

6.9.1 CE Mark

The product is certified for compliance to EC directive 89/336/EEC. The CE marking for the certification appears on the drive.

6.9.2 C-Tick Mark

The product complies with the following Australian EMC standard.

Limits and methods of measurement of radio disturbance characteristics of information technology equipment, AS/NZS 3548:1995 Class B.

6.10 Safety

6.10.1 UL and CSA approval

The product is qualified per UL (Underwriters Labratory) 1950 Third Edition and CAN/CSA C22.2 No.950-M95 Third Edition, for the use in Information Technology Equipment, including Electric Business Equipment. The UL Recognition, or the CSA certification, is maintained for the product life. The UL and C-UL recognition mark • • or CSA monogram for CSA certification • • appears on the drive.

6.10.2 IEC compliance

All DJSA-XXX drives comply with IEC 950:1991 +A1-4.

6.10.3 German Safety Mark

All DJSA-XXX drives are approved by TUV on Test Requirement: EN 60950:1992+A1-4, but the GS mark has not been obtained.

6.10.4 Flammability

The printed circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better except minor mechanical parts.

6.10.5 Secondary circuit protection

This product utilizes printed circuit wiring that must be protected against the possibility of sustained combustion due to circuit or component failures as defined in C-B 2-4700-034 (Protection Against Combustion). Adequate secondary over current protection is the responsibility of the using system.

The user must protect the hard disk drive from its electrical short circuit problem. A 10 amp limit is required for safety purpose.

6.11 Packaging

Drives will be packed in ESD protective bags and shipped in appropriate containers.

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7.0 Electrical interface specifications

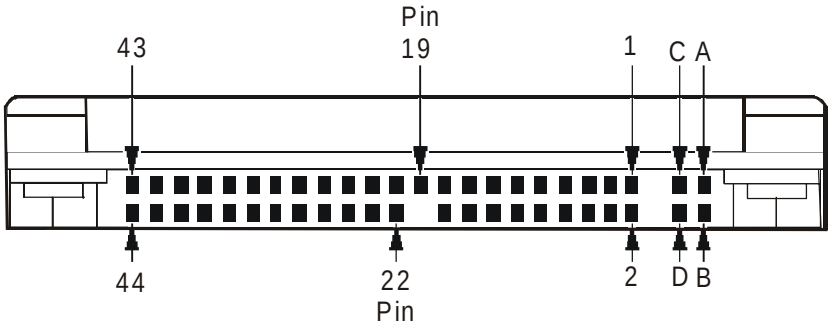
7.1 Cabling

The maximum cable length from the host system to the hard disk drive shall not exceed 18 inches.

7.2 Interface connector

The signal connector for AT attachment is designed to mate with the 50 pin plug specified in Annex A, Connectors and Cable Assembly, of the ATA/ATAPI-5 document.

The figure below and Figure 6.5.2 on page 31 show the connector location and physical pin location.



Note 1: Pin position 20 is left blank for correct connector insertion.
Note 2: Pin positions A, B, C, and D are used for drive address setting. (Refer to Figure 45 on page 57 for correct address setting.)

Figure 32. Interface connector pin assignments

7.3 Signal definitions

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	–RESET	I	TTL	02	GND		
03	DD07	I/O	3–state	04	DD08	I/O	3–state
05	DD06	I/O	3–state	06	DD09	I/O	3–state
07	DD05	I/O	3–state	08	DD10	I/O	3–state
09	DD04	I/O	3–state	10	DD11	I/O	3–state
11	DD03	I/O	3–state	12	DD12	I/O	3–state
13	DD02	I/O	3–state	14	DD13	I/O	3–state
15	DD01	I/O	3–state	16	DD14	I/O	3–state
17	DD00	I/O	3–state	18	DD15	I/O	3–state
19	GND			(20)	Key		
21	DMARQ	O	3–state	22	GND		
23	–DIOW(*)	I	TTL	24	GND		
25	–DIOR(*)	I	TTL	26	GND		
27	IORDY(*)	O	OD	28	CSEL	I	TTL
29	–DMACK	I	TTL	30	GND		
31	INTRQ	O	3–state	32	–IOCS16(*)	O	OD
33	DA01	I	TTL	34	–PDIAG	I/O	OD
35	DA00	I	TTL	36	DA02	I	TTL
37	–CS0	I	TTL	38	–CS1	I	TTL
39	–DASP	I/O	OD	40	GND		
41	+ 5V logic	power		42	+ 5V motor	power	
43	GND			44	(reserved)		

Notes:

1. *"O" designates an output from the Drive.*
2. *"I" designates an input to the Drive.*
3. *"I/O" designates an input/output common.*
4. *"OD" designates an Open-Drain output.*
5. *The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the Host decides to allow a DMA burst, if the Ultra DMA transfer mode was previously chosen via SetFeatures. The Drive becomes aware of this change upon assertion of the -DMACK line. These lines revert back to their original definitions upon the deassertion of DMACK at the termination of the DMA burst.*
6. *"power" designates a power supply to the drive.*
7. *"reserved" designates reserved pins which must be left unconnected.*

Figure 33. Table of signals

	Special Definition (for Ultra DMA)	Conventional Definition
Write Operation	–DDMARDY	IORDY
	HSTROBE	–DIOR
	STOP	–DIOW
Read Operation	–HDMARDY	–DIOR
	DSTROBE	IORDY
	STOP	–DIOW

Figure 34. Special signal definitions for Ultra DMA

7.4 Signal descriptions

DD00–DD15

A 16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00–15, are used for data transfer. These are 3-state lines with 24 mA current sink capability.

DA00–DA02

These are addresses used to select the individual register in the HDD.

-CS0

The chip select signal generated from the Host address bus. When active, one of the Command Block Registers [Data, Error (Features when written), Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status (Command when written) register] can be selected.

-CS1

The chip select signal generated from the Host address bus. When active, one of the Control Block Registers [Alternate Status (Device Control when written) and Drive Address register] can be selected.

-RESET

This line is used to reset the HDD. It shall be kept at a Low logic state during power up and kept High thereafter.

-DIOW

The rising edge of this signal holds data from the data bus to a register or data register of the HDD.

-DIOR

When this signal is low it enables data from a register or data register of the drive onto the data bus. The data on the bus shall be latched on the rising edge of -DIOR.

INTRQ

The interrupt is enabled only when the drive is selected and the host activates the -IEN bit in the Device Control Register. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. The IRQ is reset to zero by a host read of the status register or a write to the Command Register. This signal is a 3-state line with 24 mA of sink capability.

-IOCS16

A signal indicating to the host that a 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

-DASP

This is a time-multiplexed signal which indicates that a drive is active or that device 1 is present. This signal is driven by an Open-Drain driver and internally pulled up to 5 volts through a 10 kΩ resistor. During a Power-On initialization or after -RESET is negated, -DASP shall be asserted by Device 1 within 400 ms to indicate that device 1 is present. Device 0 shall allow up to 450 ms for device 1 to assert -DASP. If device 1 is not present, device 0 may assert -DASP to drive an LED indicator. The -DASP signal shall be negated following acceptance of the first valid command by device 1. Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.

-PDIAG

This signal shall be asserted by device 1 to indicate to device 0 that it has completed the diagnostics. This line is pulled up to 5 volts in the HDD through a 10 kΩ resistor.

Following a Power On Reset—software reset or -RESET—drive 1 shall negate -PDIAG within 1 ms (to indicate to device 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy and is able to provide status.

Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate -PDIAG within 1 ms to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Device 1 should clear BSY before asserting -PDIAG, as -PDIAG is used to indicate that device 1 has passed its diagnostics and is ready to post status. If -DASP was not asserted by device 1 during reset initialization, device 0 shall post its own status immediately after it completes diagnostics and clears the device 1 Status register to 00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

CSEL (Cable Select)

This signal is monitored to determine the drive address (master or slave) when the jumper on the interface connector is at Position-3.

When CSEL is at ground or is at a low level the HDD works as a Master. If CSEL is open or is at a logical high level the HDD works as a Slave.

The signal level of CSEL to one HDD should be different from the signal level to another HDD on the same AT interface cable to avoid master-master or slave-slave configurations.

KEY

Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion.

IORDY

This signal is an indication to the host that the drive is ready to complete the current I/O cycle. This line is driven low at the falling edge of -DIOR or -DIOW when HDD needs some additional WAIT cycle(s) to extend the PIO cycle. This line can be connected to the host IORDY signal in order to insert a WAIT state(s) into the host PIO cycle. This signal is an Open-Drain output with 24 mA sink capability.

5V Power

There are two input pins for the +5 V power supply. One is the "+5 V Logic" input pin and the second is the "+5 V Motor" input pin. These two input pins are tied together within the drive.

-DMACK

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

This signal is internally pulled up to 5 Volt through a 15 kΩ resistor with a resistor tolerance value of –50% to +100%.

DMARQ

This signal is used for DMA data transfers between the host and drive. It shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW signals. This signal is used in a handshake mode with -DMACK. This signal is a 3-state line with 24 mA sink capability and internally pulled down to GND through a 10 kΩ resistor.

-HDMARDY (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal -HDMARDY is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate -HDMARDY to pause an Ultra DMA data in transfer.

HSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD (15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

STOP (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The STOP signal shall be asserted by the host prior to initiation of an Ultra DMA burst. A STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

-DDMARDY (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal -DDMARDY is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate -DDMARDY to pause an Ultra DMA data out transfer.

DSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

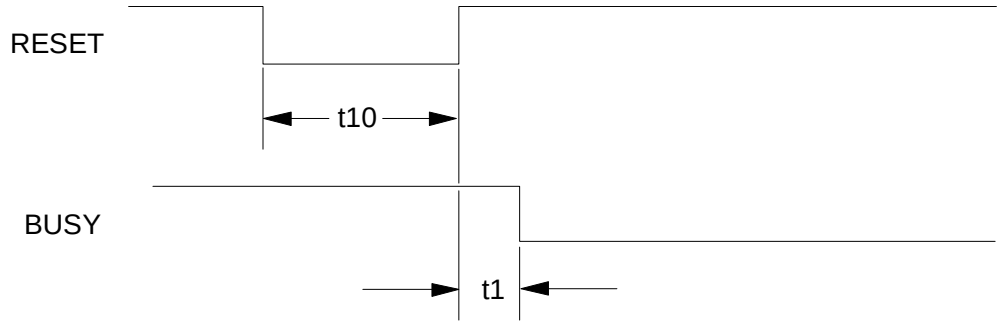
The signal DSTROBE is the data in strobe signal from the device for an Ultra DMA data in transfer. Both the rising and the falling edge of DSTROBE latch the data from DD (15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

7.5 Interface logic signal levels

The interface logic signals have the following electrical specifications:

Inputs :	Input High Voltage	2.0 V min./5.5 V max.
	Input Low Voltage	–0.5 V min./0.8 V max.
Outputs :	Output High Voltage	2.4 V min.
	Output Low Voltage	0.5 V max.
Current :	Driver Sink Current	24 mA min.
	Driver Source Current	–400 uA min.

7.6 Reset timings

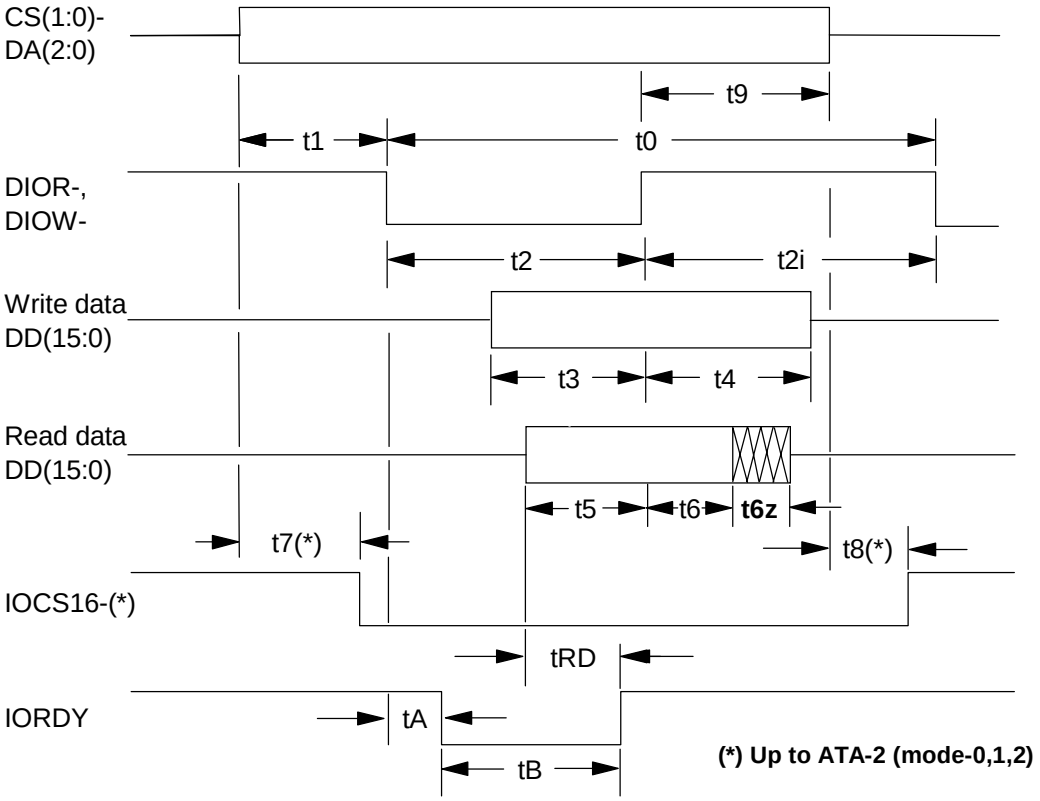


	PARAMETER DESCRIPTION	Min. (µs)	Max. (µs)
t1	RESET high to Not BUSY	–	9.5
t10	RESET low width	25	–

Figure 35. System reset timings

7.7 PIO timings

The PIO cycle timings meet Mode 4 of the ATA-5 description.

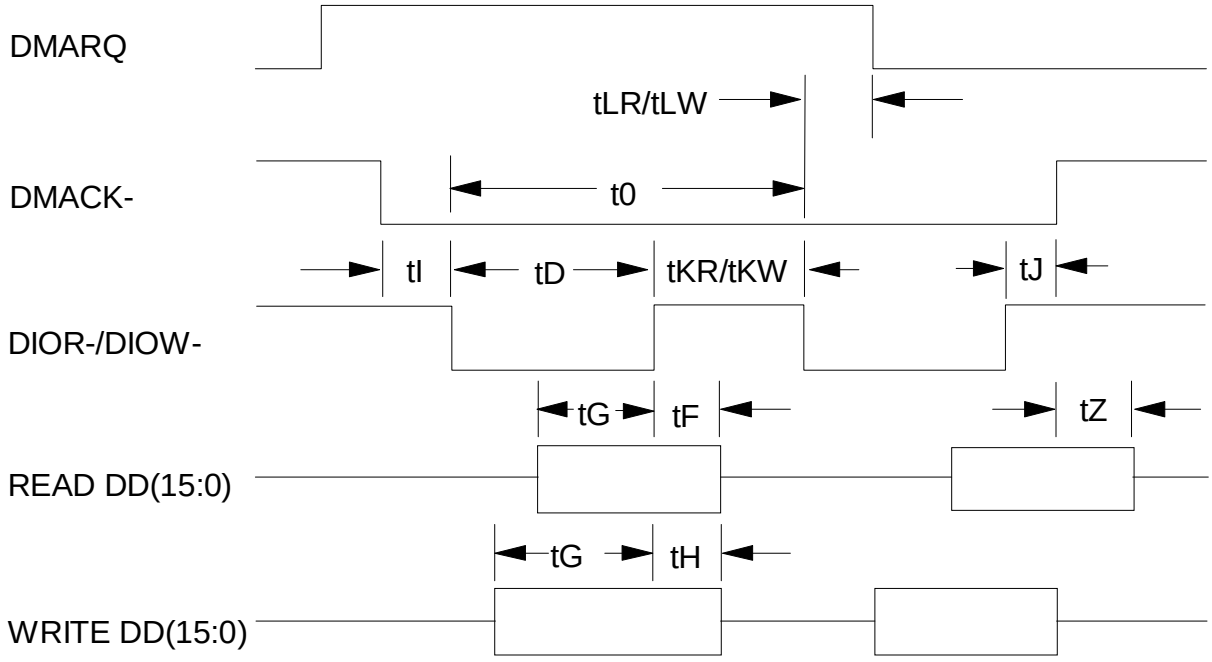


	PARAMETER DESCRIPTION	MIN (ns)	MAX. (ns)
t0	Cycle time	120	–
t1	Address valid to DIOR-/DIOW- setup	25	–
t2	DIOR-/DIOW- pulse width	70	–
t2i	DIOR-/DIOW- recovery time	25	–
t3	DIOW- data setup	20	–
t4	DIOW- data hold	10	–
t5	DIOR- data setup	20	–
t6	DIOR- data hold	5	–
t6z	DIOR- data tristate	–	30
t7(*)	Address valid to IOCS16- assertion	–	40
t8(*)	Address valid to IOCS16- released	–	30
t9	DIOR-/DIOW- to address valid hold	10	–
tRD	Read data valid to IORDY active	0	–
tA	IORDY setup time	–	35
tB	IORDY pulse width	–	1,250

Figure 36. PIO cycle timings

7.8 Multiword DMA timings

The Multiword DMA timings meet Mode 2 of the ATA-3 description.



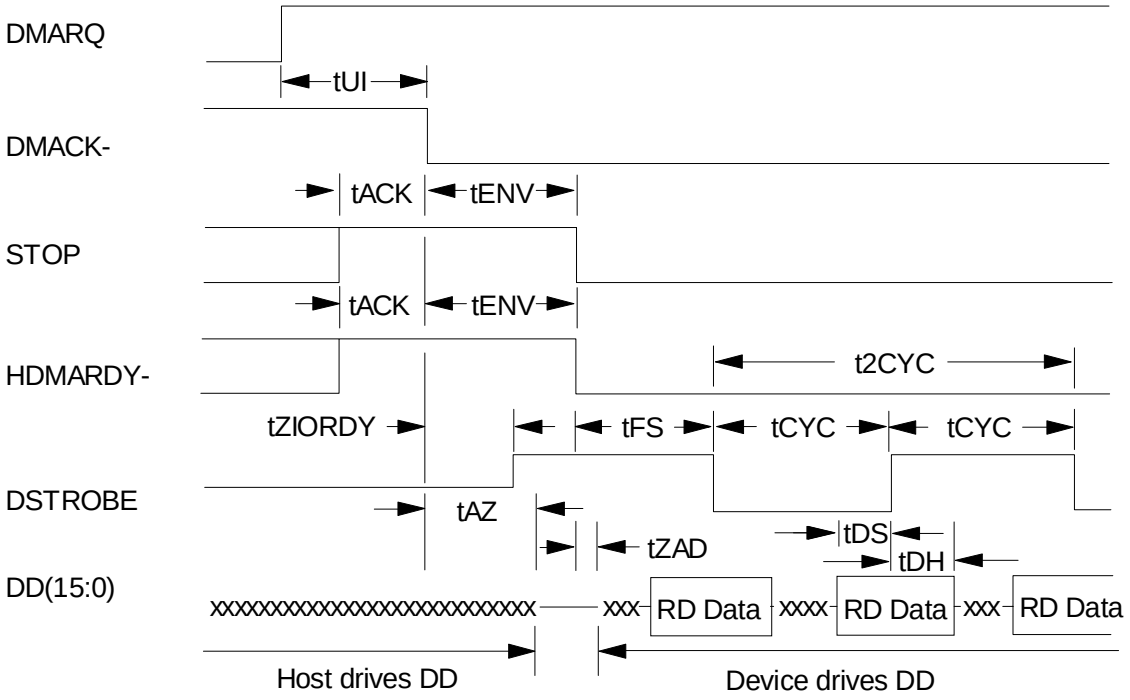
	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
tD	DIOR-/DIOW- asserted pulse width	70	–
tE	DIOR- data access	–	50
tF	DIOR- data hold	5	–
tG	DIOR-/DIOW- data setup	20	–
tH	DIOW- data hold	10	–
tI	DMACK- to DIOR-/DIOW- setup	0	–
tJ	DIOR-/DIOW- to DMACK- hold	5	–
tKR/tKW	DIOR- negated pulse width / DIOW- negated pulse width	25	–
tLR/tLW	DIOR- to DMARQ delay / DIOW- to DMARQ delay	–	35
tZ	DMACK- to read data released	–	25

Figure 37. Multiword DMA cycle timings

7.9 Ultra DMA timings

The Ultra DMA timings meet Mode 0, 1, 2, 3, and 4 of the Ultra DMA Protocol.

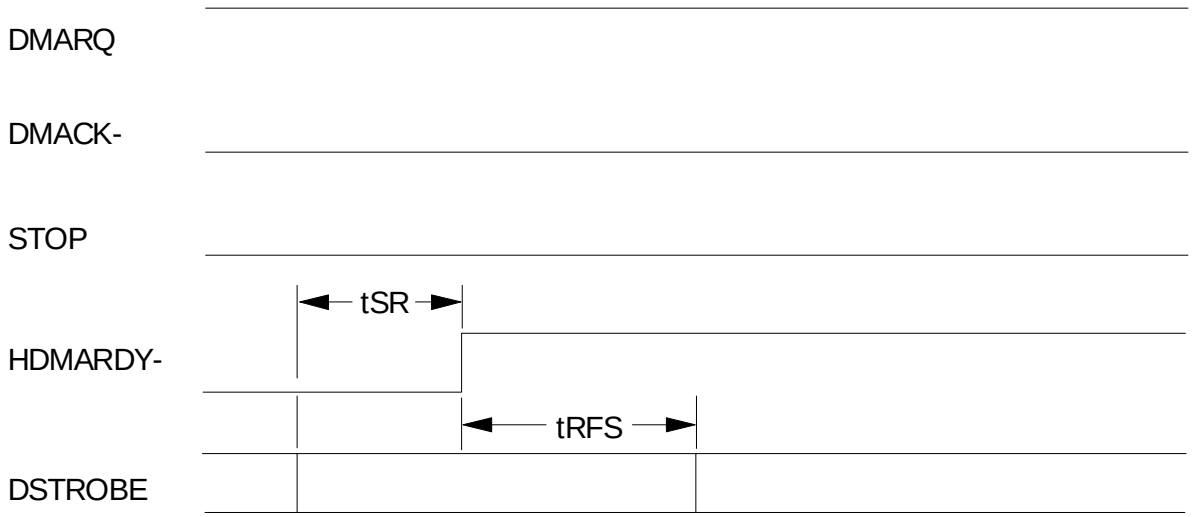
7.9.1 Initiating Read DMA



	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tUI	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–
tACK	Setup time for DMACK-	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–
tFS	First DSTROBE time	0	230	0	200	0	170	0	130	0	120
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–
t2CYC	Two cycle time	230	–	154	–	115	–	86	–	57	–
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10
tZAD	Drivers to assert	0	–	0	–	0	–	0	–	0	–
tDS	Data setup time at host	15	–	10	–	7	–	7	–	5	–
tDH	Data hold time at host	5	–	5	–	5	–	5	–	5	–

Figure 38. Ultra DMA cycle timing (Initiating Read)

7.9.2 Host Pausing Read DMA

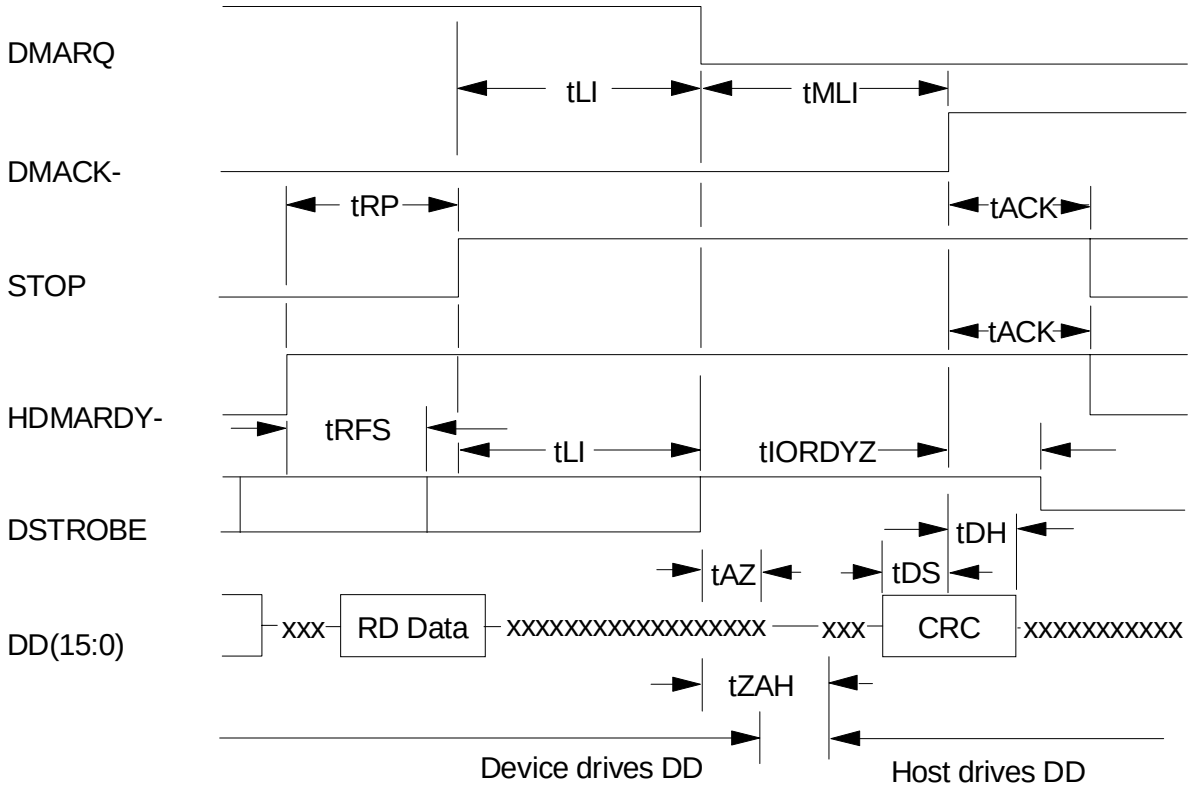


	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSR	DSTROBE to HDMARDY- time	–	50	–	30	–	20	–	–	–	–
tRFS	HDMARDY- to final DSTROBE time	–	75	–	70	–	60	–	60	–	60

Note: When a host does not satisfy the tSR timing, the host should be ready to receive two more data words after HDMARDY-.

Figure 39. Ultra DMA cycle timings (Host Pausing Read)

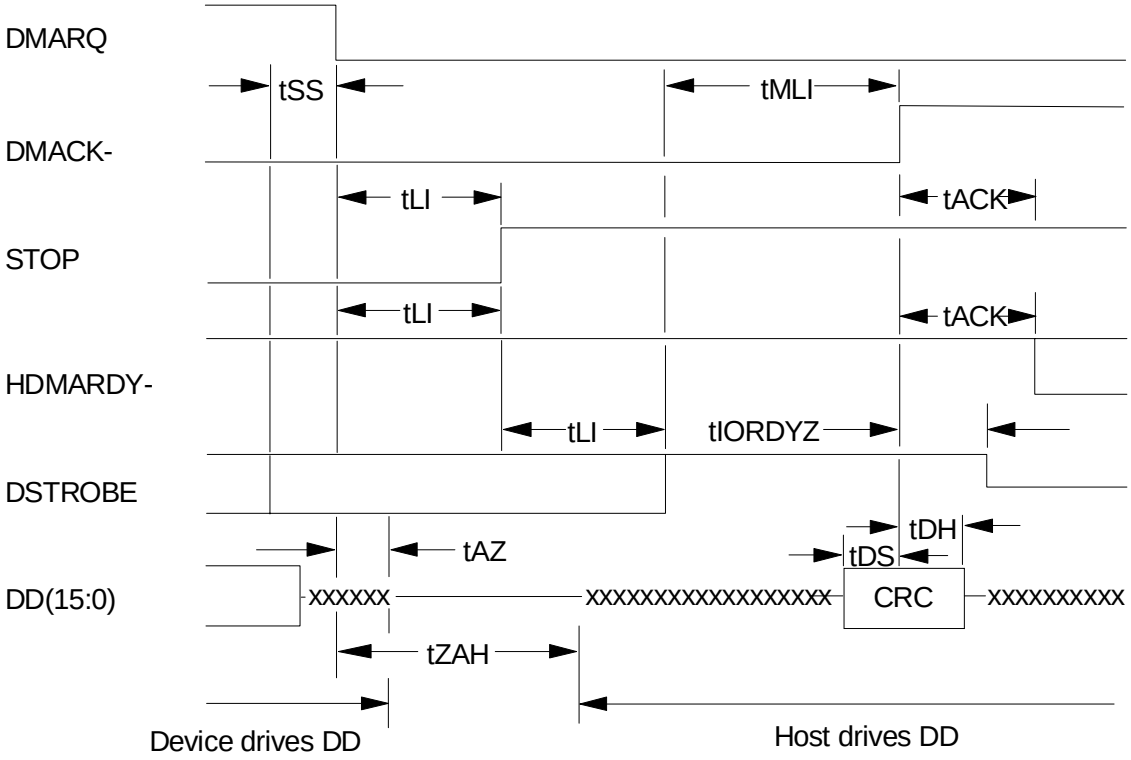
7.9.1 Host Terminating Read DMA



	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tRFS	HDMARDY- to final DSTROBE time	–	75	–	70	–	60	–	60	–	60
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10
tZAH	Minimum delay time required for output	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20

Figure 40. Ultra DMA cycle timing (Host Terminating Read)

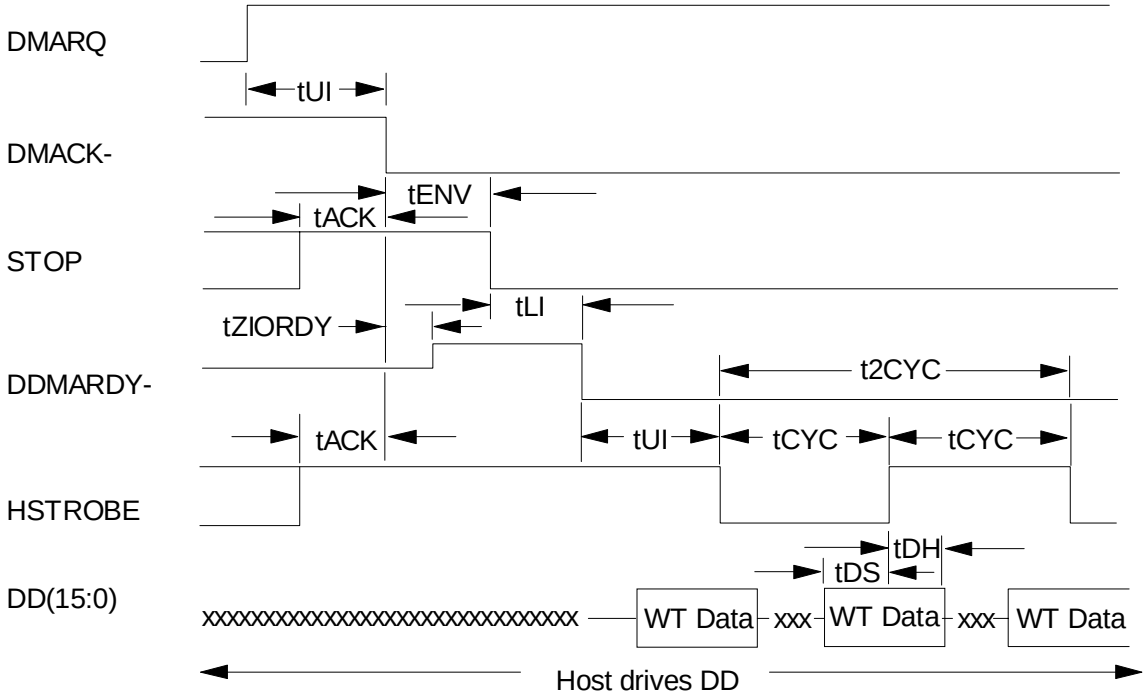
7.9.2 Device Terminating Read DMA



	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSS	Time from DSTROBE edge to negation of DMARQ	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10
tZAH	Maximum delay time required for output	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20

Figure 41. Ultra DMA cycle timings (Device Terminating Read)

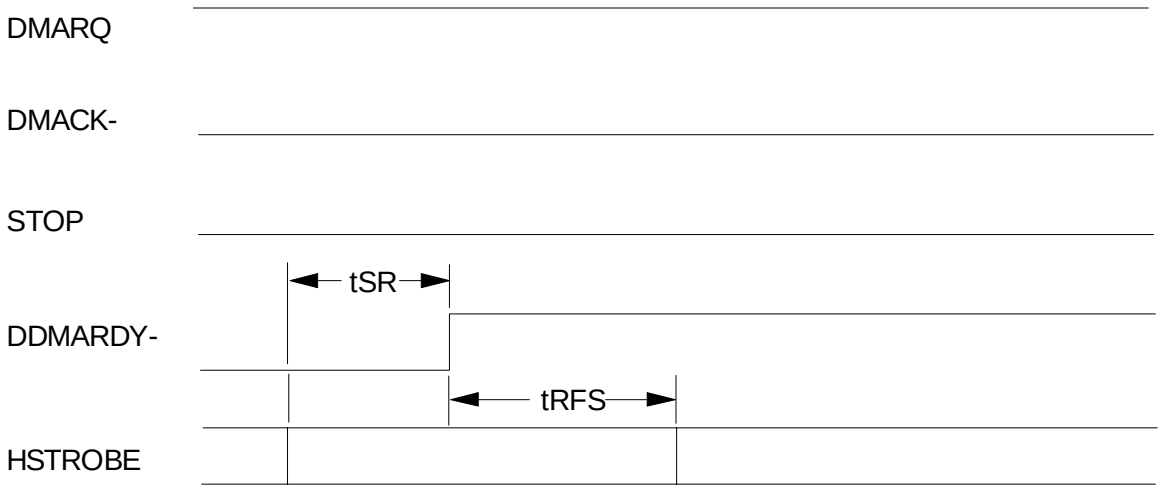
7.9.3 Initiating Write DMA



	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tUI	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–
tACK	Setup time for DMACK-	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–
t2CYC	Two cycle time	230	–	154	–	115	–	86	–	57	–
tDS	Data setup time at device	15	–	10	–	7	–	7	–	5	–
tDH	Data Hold time at device	5	–	5	–	5	–	5	–	5	–

Figure 42. Ultra DMA cycle timings (Initiating Write)

7.9.4 Device Pausing Write DMA

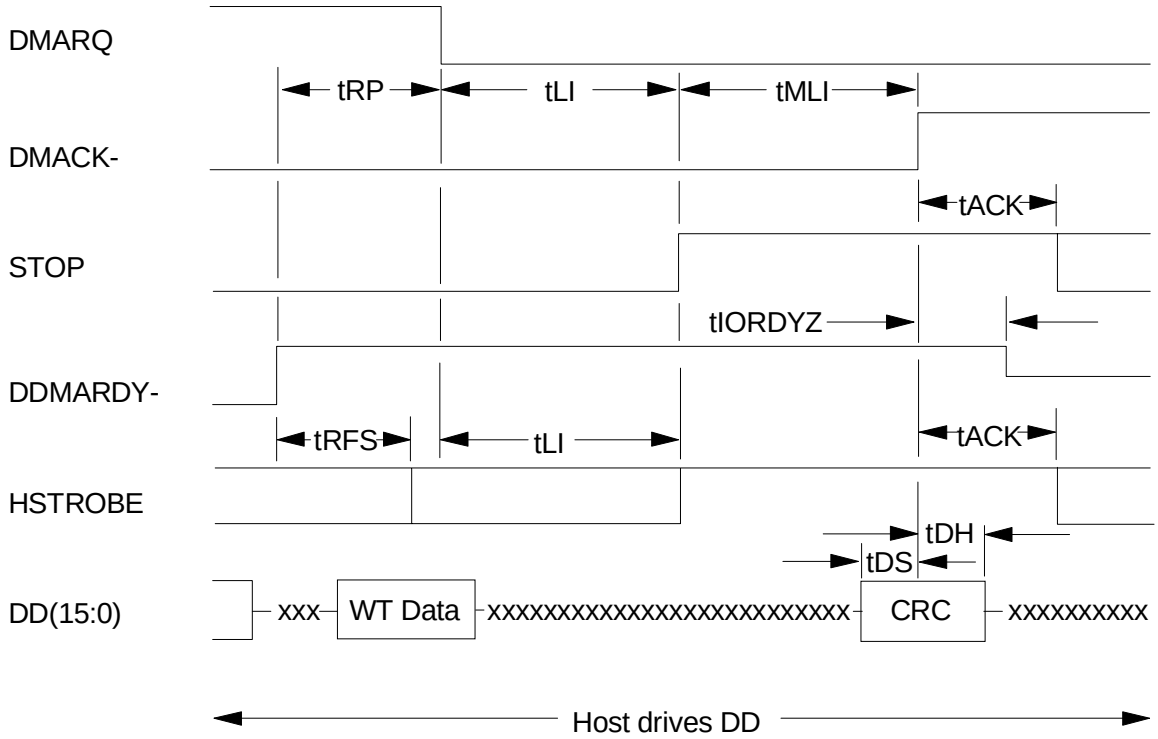


	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSR	HSTROBE to DDMARDY- time	–	50	–	30	–	20	–	–	–	–
tRFS	DDMARDY- to final HSTROBE time	–	75	–	70	–	60	–	60	–	60

Note: When a device does not satisfy the tSR timing, the device is ready to receive two more data words after DDMARDY- *is negated.*

Figure 43. Ultra DMA cycle timings (Device Pausing Write)

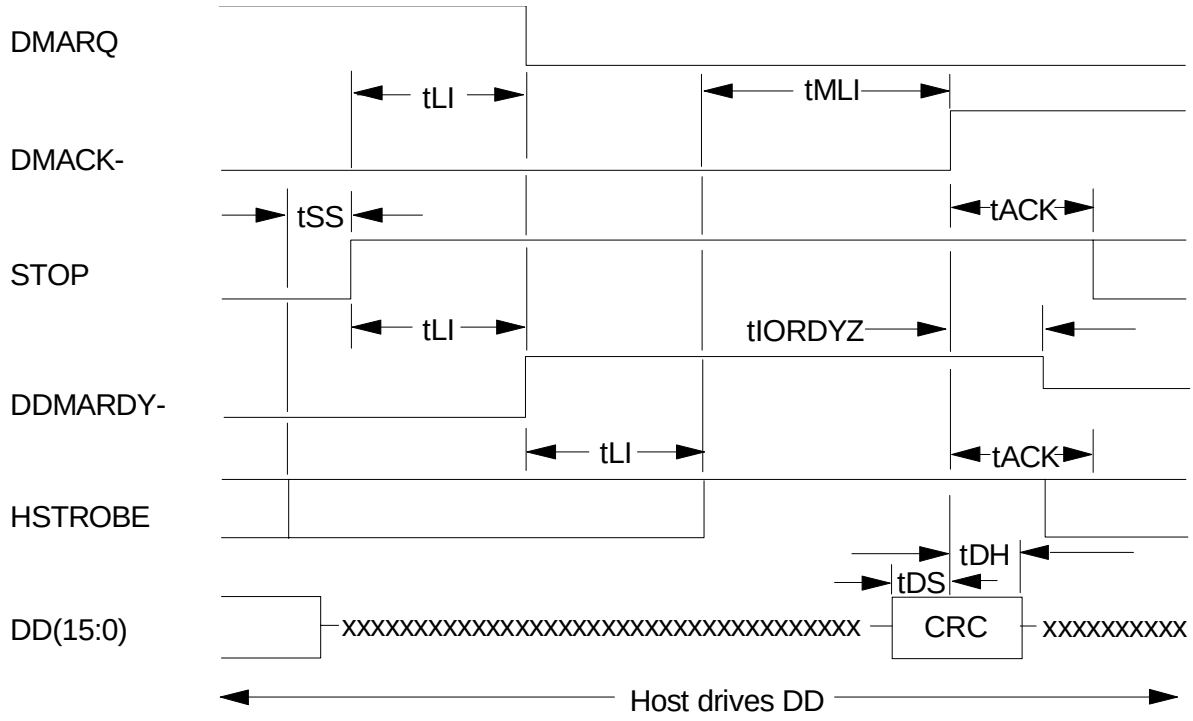
7.9.2.1 Device Terminating Write DMA



	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tRFS	DDMARDY- to final HSTROBE time	–	75	–	70	–	60	–	60	–	60
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100
tMLI	Interlocking time with minimum	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20

Figure 44. Ultra DMA cycle timings (Device Terminating Write)

7.9.3 Host Terminating Write DMA



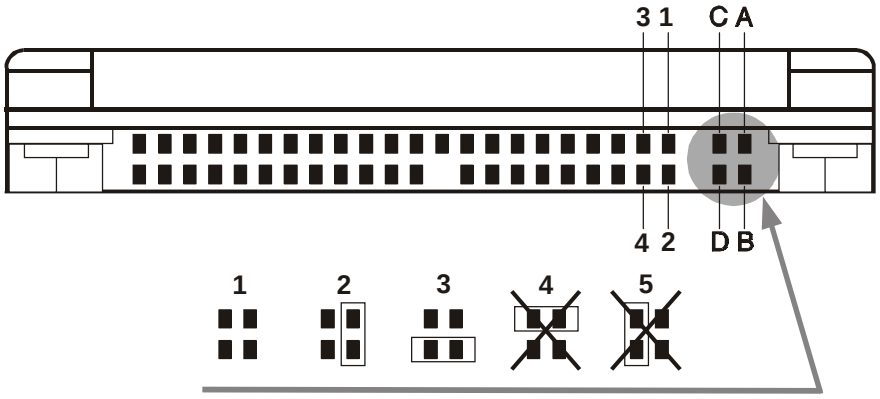
	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSS	Time from HSTROBE edge to assertion of STOP	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20

Figure 45. Ultra DMA cycle timings (Host Terminating Write)

7.10 Drive address setting

A jumper is available at the interface connector to determine the drive address. The set position of the jumper is as shown below.

Using Cable Selection, the drive address depends on the condition of pin 28 of the AT interface cable. In the case when pin 28 is ground, or low, the drive is a Master. If pin 28 is open, or logic high, the drive is a Slave.



1—Device 0 (Master)
2—Device 1 (Slave)
3—Cable Select
4—Never attach a jumper here
5—Never attach a jumper here

Note: When pin C is grounded the drive does not spin up at POR.

Figure 46. Drive address setting

7.11 Drive default address setting

The default setting of jumper at shipment is No Jumper: Device 0 (Master).

7.12 Addressing of HDD registers

The host addresses the drive through a set of registers called a Task File. These registers are mapped into the host's I/O space. Two chip select lines (-CS0 and -CS1) and three address lines (DA00–02) are used to select one of these registers, while a -DIOR or -DIOW is provided at the specified time.

The chip select line -CS0 is used to address the Command Block registers while the -CS1 is used to address Control Block registers.

The following table shows the I/ O address map.

–CS0	–CS1	DA02	DA01	DA00	–DIOR = 0 (Read)	–DIOW = 0 (Write)
					Command Block Registers	
0	1	0	0	0	Data Reg.	Data Reg.
0	1	0	0	1	Error Reg.	Features Reg.
0	1	0	1	0	Sector count Reg.	Sector count Reg.
0	1	0	1	1	Sector number Reg.	Sector number Reg.
0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
0	1	1	1	1	Status Reg.	Command Reg.
					Control Block Registers	
1	0	1	1	0	Alt. Status Reg.	Device control Reg.
1	0	1	1	1	Drive address Reg.	–

Figure 47. I/O address map

Part 2. Interface specification

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8.0 General

8.1 Introduction

This specification describes the host interface of DJSA-XXX.

The interface conforms to the Working Document of Information technology, AT Attachment with Packet Interface Extension (ATA/ATAPI-5) Revision 2 dated December 13, 1999, with certain limitations described in section 9.0, "Deviations From Standard" on page 63.

DJSA-XXX drives support the following new functions included by ATA/ATAPI-5 standards or newer standards.

- S.M.A.R.T. Error Logging and Self Test commands
- Ultra DMA/66 transfer commands

DJSA-XXX drives support the following functions as Vendor Specific Functions.

- Address Offset Feature
- Format Unit Function
- ENABLE/DISABLE DELAYED WRITE
- SENSE CONDITION command

8.2 Terminology

Device	Device indicates DJSA-XXX
Host	Host indicates the system that the device is attached to.
First Command	The first command that is executed after the power on reset (also known as a hard reset) is the Standby mode command.
INTRQ	Interrupt request (Device or Host)

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9.0 Deviations from standard

The device conforms to the referenced specifications, with deviations described below.

The interface conforms to the Working Document of Information Technology, AT Attachment with Packet Interface Extension (ATA/ATAPI-5) Revision 2 dated December 13, 1999, with deviation as follows:

Standby Timer	Standby timer is enabled by STANDBY command or IDLE command. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is set to 109 minutes automatically.
Write Verify	WRITE VERIFY command does not include read verification after write operation. The function is the same as WRITE SECTORS command.
S.M.A.R.T. Return Status	S.M.A.R.T. RETURN STATUS subcommand does not check advisory attributes. This means that the device will not report a threshold exceeded condition unless the prefailure attributes exceed their corresponding thresholds. For example, a Power-On Hours Attribute never results in a negative reliability status.

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10.0 Registers

Addresses					Functions	
CS0–	CS1–	DA2	DA1	DA0	READ (DIOR–)	WRITE (DIOW–))
N	N	x	x	x	Data bus high imped	Not used
					Control block registers	
N	A	0	x	x	Data bus high imped	Not used
N	A	1	0	x	Data bus high imped	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	* LBA bits 0-7	* LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	* LBA bits 8-15	* LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	* LBA bits 16-23	* LBA bits 16-23
A	N	1	1	0	Device/Head.	Device/Head
A	N	1	1	0	* LBA bits 24-27	* LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Logic converntions: A = Signal asserted
N = Signal not asserted
x = Does not matter which it is

* = Mapping of registers in LBA mode

Figure 48. Register Set

Communication to or from the device is through an I/O Register that routes the input or output data to or from the registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

10.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DBQ	COR	IDX	ERR

Figure 49. Alternate Status Register

This register contains the same information as the Status Register. The only difference between this register and the Status Register is that reading the Alternate Status Register does not imply an interrupt acknowledge or a clear of a pending interrupt. See 10.13, "Status Register" on page 70 for the definition of the bits in this register.

10.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Figure 68 on page 103. All other registers required for the command must be set up before writing to the Command Register.

10.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16–23. At the end of the command, this register is updated to reflect the current LBA Bits 16–23.

The cylinder number may be from zero to the number of cylinders minus one.

10.4 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8–15. At the end of the command, this register is updated to reflect the current LBA Bits 8–15.

The cylinder number may be from zero to the number of cylinders minus one (1).

10.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command and the configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ = 1 is in the Status Register.

10.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
–	–	–	–	1	SRST	–IEN	0

Figure 50. Device Control Register

Bit Definitions

SRST (RST) Software Reset. The device is held at reset when RST = 1. Setting RST = 0 again enables the device. To ensure that the device recognizes the reset, the host must set RST = 1 and wait for at least 5 microseconds before setting RST = 0.

-IEN Interrupt Enable. When IEN = 0, and the device is selected, the device interrupts to the host will be enabled. When IEN = 1, or the device is not selected, the device interrupts to the host will be disabled.

10.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	–WTG	–H3	–H2	–H1	–H0	–DS1	–DS0

Figure 51. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

HIZ High Impedance. This bit is not a device and will always be in a high impedance state.

-WTG -Write Gate. This bit is 0 when writing to the disk device is in progress.

-H3,-H2,-H1,-H0 -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. Bit -H0 is the least significant.

-DS1 -Drive Select 1. The Drive Select bit for device 1 is active low. DS1 = 0 when device 1 (slave) is selected and active.

-DS0 -Drive Select 0. The Drive Select bit for device 0 is active low. DS0 = 0 when device 0 (master) is selected and active.

10.8 Device/Head Register

Device/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 52. Device/Head Register

This register contains the device and head numbers.

Bit Definitions

L Binary encoded address mode select. When L = 0 , addressing is by CHS mode. When L = 1, addressing is by LBA mode.

DRV Device. When DRV = 0, device 0 (master) is selected. When DRV = 1, device 1 (Slave) is selected.

HS3,HS2,HS1,HS0 Head Select. These four bits indicate the binary encoded address of the head. Bit HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head. The head number may be from zero to the number of heads minus one. In LBA mode, HS3 through HS0 contain bits 24–27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24–27.

10.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 53. Error Register

This register contains the status from the last command executed by the device or a diagnostic code. At the completion of any command, except Execute Device Diagnostic, the contents of this register are always valid even if ERR = 0 is in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Figure 56 on page 73 for the definitions.

Bit Definitions

ICRCE (CRC) Interface CRC Error. When CRC = 1 it indicates that a CRC error has occurred on the data bus during a Ultra DMA transfer.

UNC Uncorrectable Data Error. When UNC = 1 it indicates that an uncorrectable data error has been encountered.

IDNF (IDN) ID Not Found. When IDN = 1 it indicates that the requested sector's ID field could not be found.

ABRT (ABT) Aborted Command. When ABT = 1 it indicates that the requested command has been aborted due to a device status error or an invalid parameter in an output register.

TK0NF (T0N) Track 0 Not Found. When T0N = 1 it indicates that track 0 was not found during a Recalibrate command.

AMNF (AMN) Address Mark Not Found. When AMN = 1 it indicates that the data address mark has not been found after finding the correct ID field for the requested sector.

10.10 Features Register

This register is command specific. This register is used with the Set Features command, the S.M.A.R.T. Function Set command, and the Format Unit command.

10.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined differently on some commands. These definitions are given in 13.0, “Command descriptions” on 103.

10.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0–7. At the end of the command, this register is updated to reflect the current LBA Bits 0–7.

10.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

Figure 54. Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY Busy. Bit BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

DRDY (RDY) Device Ready. When bit RDY=1 it indicates that the device is capable of responding to a command. Bit RDY will be set to 0 during power on until the device is ready to accept a command.

DF Device Fault. It DF=1 it indicates that the device has detected a write fault condition. Bit DF is set to 0 after the Status Register is read by the host.

DSC Device Seek Complete. If DSC=1 it indicates that a Seek has completed and the device head is settled over a track. Bit DSC is set to 0 by the device just before a Seek begins. When an error occurs, this bit is not changed until the Status Register is read by the hos and at that time the bit again indicates the current Seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of the drive not spinning up.

DRQ Data Request. Bit DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.

CORR (COR) Corrected Data. Corrected Data is always = 0.

IDX Index. Bit IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX bit for timing purposes.

ERR Error. Bit ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets bit ERR=0 when the next command is received from the host.

11.0 General operation descriptions

11.1 Reset response

ATA has the following three types of resets:

Power On Reset (POR)	The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametric, and sets default values.
Hard Reset (Hardware Reset)	The RESET signal is negated in the ATA Bus. The device resets the interface circuitry and sets the default values.
Soft Reset (Software Reset)	The SRST bit in the Device Control Register is set and then is reset. The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in Figure 54 on page 72.

	POR	hard reset	soft reset
Aborting Host interface	–	o	o
Aborting Device operation	–	(*1)	(*1)
Initialization of hardware	o	x	x
Internal diagnostic	o	x	x
Starting or Spinning Up spindle motor	(*6)	x	x
Initialization of registers (*2)	o	o	o
DASP handshake	o	o	x
PDIAG handshake	o	o	o
Reverting programmed parameters to default • Number of CHS (set by Initialize Device Parameters) • Multiple mode • Write Cache • Delayed Write • Read look-ahead • ECC bytes • Volatile max. Address • Address offset mode	o	o	(*3)
Power mode	(*6)	(*4)	(*4)
Reset Standby timer value (*5)	o	o	o

o—execute
x—not execute

Note.
(*1). *Execute after the data in write cache has been written.*
(*2). *The default value on POR is shown in Figure 55 on page 73.*
(*3). *The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.*
(*4). *In the case of sleep mode, the device goes to standby mode. In other cases, the device does not change current mode.*
(*5). *After reset the Standby timer value is set to 109 minutes.*
(*6). *Set according to the initial power mode selection.*

Figure 55. Reset response table

11.1.1 Register initialization

After a power on, a hard reset, or a software reset, the register values are initialized as shown in the table below.

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	A0h
Status	50h
Alternate Status	50h

Figure 56. Default Register Values

As a result of carrying out an Execute Device Diagnostic command or being powered on, or if a hard reset occurs—the system generates an Error Register diagnostic code. See the table below for a description of the various codes.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

Figure 57. Diagnostic Codes

11.2 Diagnostic and Reset considerations

The Set Max password, the Set Max security mode and the Set Max unlock counter are not retained over a Power On Reset but are retained over a Hard Reset or Soft Reset.

For each Reset and Execute Device Diagnostic, the diagnostic is done as follows:

Power On Reset, Hard Reset DASP– is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP– to indicate device activity. If Device 1 is not present, Device 0 does not Assert DASP– at POR.

Soft Reset If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors; otherwise, Device 0 shall simply reset and clear the BSY bit. DASP– is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command; otherwise, Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP– is asserted by Device 0 (and Device 1 if it is present) in order to indicate that the device is active.

In each case—**Power On Reset [Hard Reset**], **Soft Reset**, and the **Execute Device Diagnostic** command—the Device 0 Error register value is interpreted using the table below.

Device 1 present?	PDIAG– Asserted?	Device 0 Passed		Error Register
Yes	Yes	Yes		01h
Yes	Yes	No		0xh
Yes	No	Yes		81h
Yes	No	No		8xh
No	(not read)	Yes		01h
No	(not read)	No		0xh

The "x" indicates the appropriate Diagnostic Code for the Power on, RESET–, Soft Reset, or Device Diagnostic error.

Figure 58. Reset error register values

11.3 Power-off considerations

11.3.1 Load/Unload

Load/Unload is a functional mechanism of the HDD. It is controlled by the drive micro code. Specifically, unloading of the heads is invoked by the following commands.

Command	
Standby	UL -> Comp.
Standby Immediate	UL -> Comp.
Sleep	UL -> Comp.

Reset	
Soft Reset	UL -> Rdy
Hard Reset	UL -> Rdy

x —means "don't care"

"Imme." —means "immediate"

"Comp" —means "complete"

"UL" —means "unload"

"Rdy" —means "interface ready"

(*1) Load/Unload condition is not changed by Soft Reset.

The microcode revision is referred to words 23–26 [eight characters in ASCII code] in the "Identify Device" paragraph 13.7 on page 114.

Figure 59. Device behavior by ATA commands.

Load/unload is also invoked as one of the idle modes of the drive.

The specified start/stop life of the product assumes that load/unload is operated normally, NOT in emergency mode.

11.3.2 Emergency unload

When HDD power is interrupted while the heads are still loaded, the microcode cannot operate and the normal 5V power is unavailable to unload the heads. In this case, normal unload is not possible, so the heads are unloaded by routing the back-EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case, and the unload process is inherently less controllable without a normal seek current profile.

Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

A single emergency unload operation is more stressful than 100 normal unloads. Use of emergency unload reduces the start/stop life of the HDD at a rate at least 100X faster than that of normal unload, and may damage the HDD.

11.3.3 Required power-off sequence

Problems can occur on most HDDs when power is removed at an arbitrary time. Examples:

- Data loss from the write buffer.
- If the drive is writing a sector, a partially-written sector with an incorrect ECC block results. The sector contents are destroyed, and reading that sector results in a hard error.
- Heads possibly land in the data zone instead of the landing zone, depending on the design of the HDD.

You may then turn off the HDD in the following order:

1. Issue Standby Immediate or sleep command.
2. Wait until COMMAND COMPLETE STATUS is returned. (It may take up to 350 ms in typical case)
3. Terminate power to HDD.

This power-down sequence should be followed for entry into any system power-down state, or system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios such as battery removal during operation.

11.4 Sector Addressing Mode

All addressing of data sectors recorded on the device's media are done by a logical sector address. The logical CHS address for the DJSA-XXX drive is different from the actual physical CHS location of the data sector on the disk media.

DJSA-XXX drives support both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. A host system must set the L bit to 1 if the host uses LBA Addressing mode.

11.4.1 Logical CHS addressing mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number, and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but cannot exceed 255 (0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 15 (0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535 (0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

LBA addressing mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

```
LBA = ((cylinder*heads_per_cylinder+heads)*sectors_per_track)+sector–1
      where heads_per_cylinder and sectors_per_track are the current
      translation mode values.
```

On LBA addressing mode, the LBA value is set to the following register.

```
Device/Head       <–––– LBA bits 27–24
Cylinder High     <–––– LBA bits 23–16
Cylinder Low      <–––– LBA bits 15– 8
Sector Number     <–––– LBA bits  7– 0
```

11.5 Power management features

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

DJSA-XXX implements the following set of functions.

1. A Standby timer
2. Idle command
3. Idle Immediate command
4. Sleep command
5. Standby command
6. Standby Immediate command

11.5.1 Power Mode

Sleep Mode The lowest power consumption when the device is powered on occurs in Sleep Mode. When in sleep mode, the device requires a reset to be activated.

Standby Mode The device interface is capable of accepting commands, but as the media may not be immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

Idle Mode Refer to 11.6, Adaptive Battery Life Extender (ABLE-3) feature.

Active Mode The device is in execution of a command or accessing the disk media with the read look-ahead function or the write cache function.

11.5.2 Power management commands

The Check Power Mode command allows a host to determine if a device is currently in, going to, or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The sleep command moves a device to sleep mode. The device's interface becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode it will enter standby mode.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

11.5.3 Standby/Sleep command completion timing

1. Confirm the completion of writing cached data in the buffer to media.
2. Unload the heads on the ramp.
3. Set the DRDY bit and the DSC bit in Status Register.
4. Set the INTRQ (completion of the command).
5. Activate the spindle break to stop the spindle motor.
6. Wait until the spindle motor is stopped.
7. Perform the post process.

11.5.4 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of the SECTOR COUNT register on Idle command or the Standby command is set to "00h", the device will automatically set the standby timer to 109 minutes.

11.5.5 Status

In the active, idle, and standby modes, the device shall have the RDY bit of the status register set. If the BSY bit is not set, the device shall be ready to accept any command.

In sleep mode, the device's interface is not active. A host shall not attempt to read the device's status or issue commands to the device.

11.5.6 Interface Capability for Power Modes

Each power mode affects the physical interface as defined in the following table:

Mode		BSY	RDY	Interface active	Media
Active		x	x	Yes	Active
Idle		o	1	Yes	Active
Standby		o	1	Yes	Inactive
Sleep		x	x	No	Inactive

Figure 60. Power conditions

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

Though the interface is inactive in sleep mode, the access to the interface registers and the validity of INTRQ is guaranteed for two seconds after the Sleep command is completed. After this period, the contents of interface registers may be lost. Since the contents of interface registers may be invalid, the host should NOT check the Status register nor the Alternate Status register prior to issuing a soft reset to wake up a device.

11.5.7 Initial Power Mode at Power On

After power on or hard reset the device goes to IDLE mode or STANDBY mode depending on the option. Refer to Part 1 of this document for the initial power mode selection.

11.6 Advanced Power Management (ABLE-3) feature

This feature provides power saving without performance degradation. The Adaptive Battery Life Extender 3 (ABLE-3) technology intelligently manages transition among power modes within the device by monitoring access patterns of the host.

This technology has three idle modes; Performance Idle mode, Active Idle mode, and Low Power Idle mode.

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands, described in the section of Set Feature command in detail.

This feature set uses the following functions:

- A SET FEATURES subcommand to enable Advanced Power Management
- A SET FEATURES subcommand to disable Advanced Power Management

The Advanced Power Management feature is independent of the Standby timer setting. If both Advanced Power Management level and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that it is time to enter the Standby state.

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 91, bits 7-0 contain the current Advanced Power Management level if Advanced Power Management is enabled.

11.6.1 Performance Idle Mode

This mode is usually entered immediately after Active mode command processing is complete, instead of conventional idle mode. In Performance Idle mode, all electronic components remain powered and full frequency servo remains operational. This provides instantaneous response to the next command. The duration of this mode is intelligently managed as described below.

11.6.2 Active Idle Mode

In this mode, power consumption is 45–55% less than that of Performance Idle mode. Additional electronics are powered off, and the head is parked near the mid-diameter of the disk without servoing. Recovery time to Active mode is about 20 ms.

11.6.3 Low Power Idle Mode

Power consumption is 60–65% less than that of Performance Idle mode. The heads are unloaded on the ramp, however the spindle is still rotated at the full speed. Recovery time to Active mode is about 300 ms.

11.6.4 Transition Time

The transition time is dynamically managed by users recent access pattern, instead of fixed times. The ABLE-3 algorithm monitors the interval between commands instead of the command frequency of ABLE-2. The algorithm supposes that next command will come with the same command interval distribution as the previous access pattern. The algorithm calculates the expected average saving energy and response delay for next command in several transition time case based on this assumption. And it selects the most effective transition time with the condition that the calculated response delay is shorter than the value calculated from the specified level by Set Feature Enable Adaptive Power Management command.

The optimal time to enter Active Idle mode is variable depending on the recent behavior of the user. It is not possible to achieve the same level of Power savings with a fixed entry time into Active Idle because every user’s data and access pattern is different. The optimum entry time changes over time.

The same algorithm works for entering into Low Power Idle mode and Standby mode, which consumes less power but need more recovery time switching from this mode to Active mode.

11.7 S.M.A.R.T. Function

The intent of S.M.A.R.T. is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T. devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

Since S.M.A.R.T. utilizes the internal device microprocessor and other device resources, there may be some small overhead associated with its operation. However, special care has been taken in the design of the S.M.A.R.T. algorithms to minimize the impact to host system performance. Actual impact of S.M.A.R.T. overhead is dependent on the specific device design and the usage patterns of the host system. To further ensure minimal impact to the user, S.M.A.R.T. capable devices are shipped from the device manufacturer's factory with the S.M.A.R.T. feature disabled. S.M.A.R.T. capable devices can be enabled by the system OEMs at time of system integration or in the field by after-market products.

11.7.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

11.7.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or fault condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a

degrading or fault condition existing. There is no implied linear reliability relationship corresponding to the numerical relationship between different attribute values for any particular attribute.

11.7.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

11.7.4 Threshold exceeded condition

If one or more attribute values are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

11.7.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reporting information.

11.7.6 S.M.A.R.T. operation with power management modes

It is recommended that, when a host system utilizes both the power management and S.M.A.R.T. features, the system enables the device's attribute auto save feature to allow the device's automatic attribute saving upon receipt of STANDBY IMMEDIATE or SLEEP commands. If the device has been set to utilize the standby timer, the device also saves attribute values prior to going from an Idle state to Standby state.

11.8 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to a device even if it is removed from the computer.

New commands are supported for this feature as below.

Security Set Password	('F1'h)
Security Unlock	('F2'h)
Security Erase Prepare	('F3'h)
Security Erase Unit	('F4'h)
Security Freeze Lock	('F5'h)
Security Disable Password	('F6'h)

11.8.1 Security Mode

Following security modes are provided.

Device Locked Mode	The device disables media access commands after power on. Media access commands are enabled by either a Security Unlock command or a Security Erase Unit command.
Device Unlocked Mode	The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a Security Unlock or a Security Erase Unit command.
Device Frozen Mode	The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

11.8.2 Security level

Following security levels are provided.

High level security	When the device lock function is enabled and the User Password is forgotten the device can be unlocked via a Master Password.
Maximum level security	When the device lock function is enabled and the User Password is forgotten then only the Master Password with a Security Erase Unit command can unlock the device. Then user data is erased.

11.8.3 Password

This function can have two types of passwords as described below.

Master Password	When the Master Password is set, the device does NOT enable the Device Lock Function, and the device CANNOT be locked with the Master Password, but the Master Password can be used for unlocking the locked device.
User Password	The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and then the device is locked on the next power on reset or hard reset.

The system manufacturer/dealer who intends to enable the device lock function for end users must set the master password even if only single level password protection is required. Otherwise, the 'default' master password which is set by IBM can unlock a device that is locked with a user password.

11.8.4 Master Password Revision Code

This Master Password Revision Code is set by Security Set Password command with the master password. And this revision code field is returned in the Identify Device command word 92. The valid revision codes are 0001h to FFFEh. The default value of Master Password Revision Code is FFFEh. Values 0000h and FFFFh are reserved.

11.8.5 Operation example

11.8.5.1 Master Password setting

The system manufacturer/dealer can set a new Master Password from default Master Password using the Security Set Password command, without enabling the Device Lock Function.

11.8.5.2 User Password setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

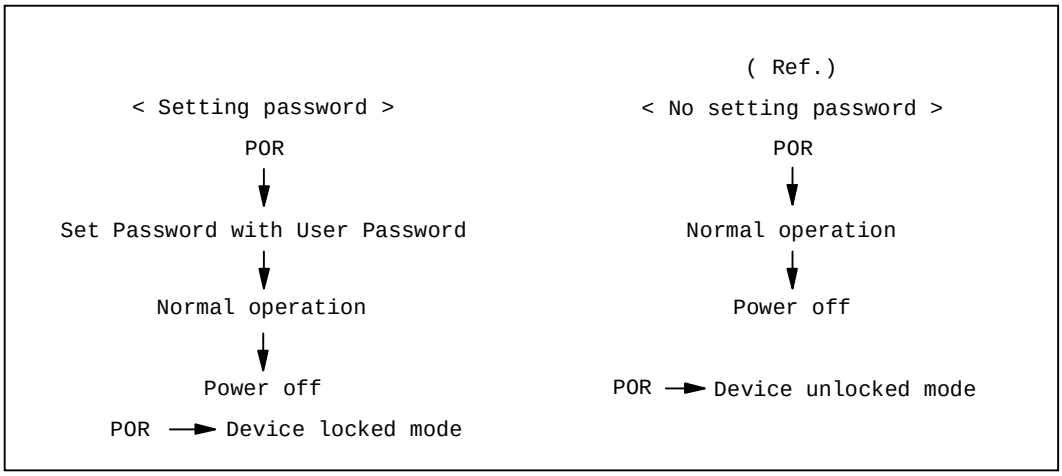

Figure 61. Initial setting

11.8.5.3 Operation from POR after user password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.

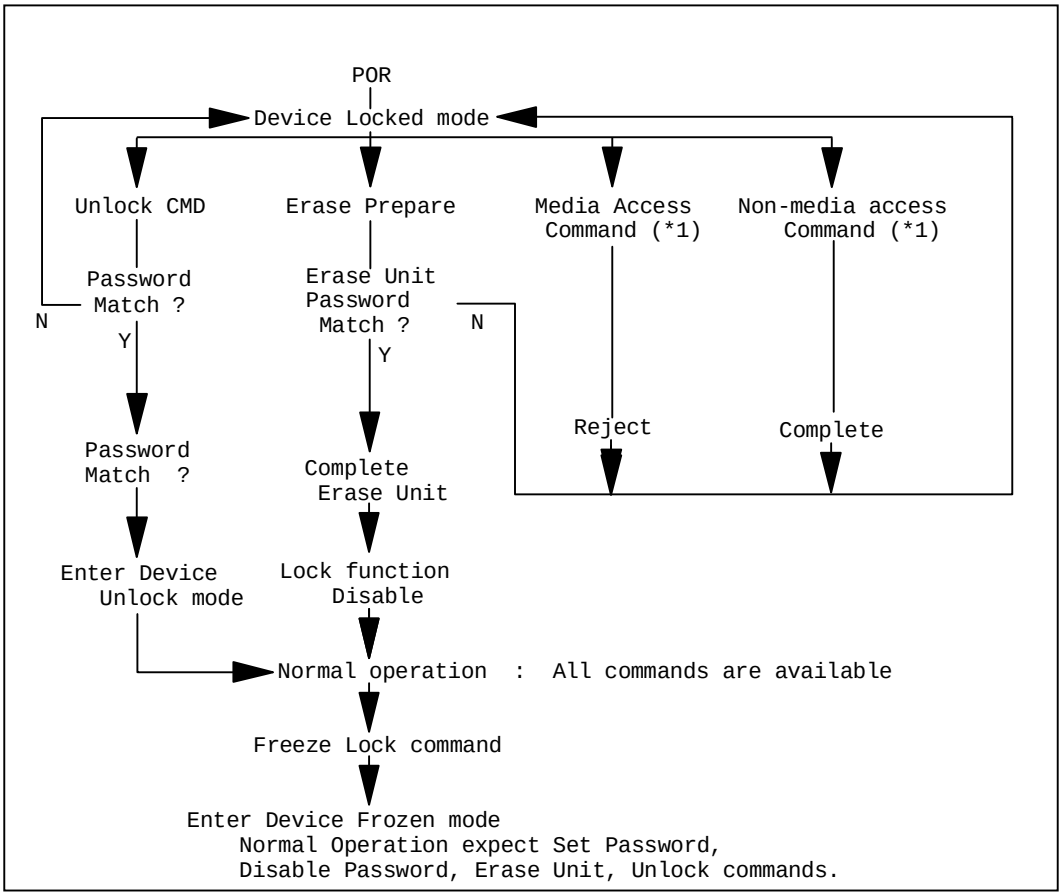

Figure 62. Usual operation

11.8.5.4 User Password lost

If the User Password is forgotten and High level security is set, the system user can't access any data. However the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

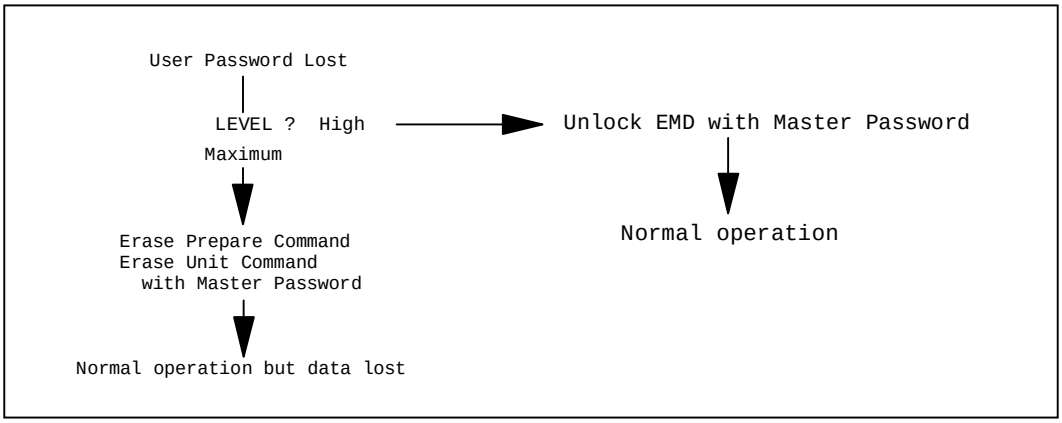

Figure 63. Password lost

11.8.5.5 Attempt limit for the SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit which helps to prevent a user from attempting to unlock the drive with various passwords numerous times.

The device counts the password mismatch. If the password does not match, the device counts it without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit (bit 4) of Word 128 in Identify Device information is set, and then the SECURITY ERASE UNIT command and the SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

11.8.6 Command table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Command	Device Locked Mode	Device Unlockeod Mode	Device Frozen Mode
Check Power Mode	o	o	o
Enable/Disable Delayed Write	o	o	o
Execute Device Diagnostic	o	o	o
Flush Cache	o	o	o
Format Track	x	o	o
Format Unit	x	o	o
Identify Device	o	o	o
Identify Device DMA	o	o	o
Idle	o	o	o
Idle Immediate	o	o	o
Initialize Device Parameters	o	o	o
Read Buffer	o	o	o
Read DMA (w/o retry)	x	o	o
Read DMA (w/retry)	x	o	o
Read Long (w/o retry)	x	o	o
Read Long (w/retry)	x	o	o
Read Multiple	x	o	o
Read Native Max ADDRESS	o	o	o
Read Sector(s) (w/o retry)	x	o	o
Read Sector(s) (w/retry)	x	o	o
Read Verify Sector(s) (w/o retry)	x	o	o
Read Verify Sector(s) (w/retry)	x	o	o
Recalibrate	o	o	o
Security Disable Password	x	o	x
Security Erase Prepare	o	o	o
Security Erase Unit	o	o	x
Security Freeze Lock	x	o	o
Security Set Password	x	o	x
Security Unlock	o	o	x
Seek	o	o	o
Sense Condition	o	o	o
Set Features	o	o	o
Set Max ADDRESS	o	o	o
Set Max FREEZE LOCK	o	o	o
Set Max LOCK	o	o	o
Set Max SET PASSWORD	o	o	o
Set Max UNLOCK	o	o	o
Set Multiple Mode	o	o	o
Sleep	o	o	o
S.M.A.R.T. Disable Operations	o	o	o

Figure 64. Command table for device lock operation (1 of 2)

Command	Device Locked Mode	Device Unlocked Mode	Device Frozen Mode
S.M.A.R.T. Enable/Disable Attribute Autosave	o	o	o
S.M.A.R.T. Enable Operations	o	o	o
S.M.A.R.T. Execute Off-line Immediate	o	o	o
S.M.A.R.T. Read Attribute Values	o	o	o
S.M.A.R.T. Read Attribute Thresholds	o	o	o
S.M.A.R.T. Return Status	o	o	o
S.M.A.R.T. Save Attribute Values	o	o	o
Standby	o	o	o
Standby Immediate	o	o	o
Write Buffer	o	o	o
Write DMA (w/o retry)	x	o	o
Write DMA (w/retry)	x	o	o
Write Long (w/o retry)	x	o	o
Write Long (w/retry)	x	o	o
Write Multiple	x	o	o
Write Sector(s) (w/o retry)	x	o	o
Write Sector(s) (w/o retry)	x	o	o
Write Verify	x	o	o

o—Device executes command normally
x—Device terminates command with error register of Aborted Command.

Figure 64. Command table for device lock operation (2 of 2)

11.9 Protected Area Function

Protected Area Function is to provide the 'protected area' which cannot be accessed via conventional methods. This 'protected area' is used to contain critical system data such as BIOS or system management information. The contents of the entire system main memory may also be dumped into the 'protected area' to resume after a system power off.

The LBA/CYL changed by the following commands affects the Identify Device Information.

Two commands are defined for this function.

Read Native Max ADDRESS ('F8'h)

Set Max ADDRESS ('F9'h)

Four security extension commands are implemented as subfunctions of the Set Max ADDRESS.

Set Max UNLOCK
Set Max FREEZE LOCK
Set Max LOCK
Set Max SET PASSWORD

11.9.1 Example for operation (In LBA Mode)

Assumptions :

For easier understanding the following example uses actual values for LBA, size, etc. Since it is an example, these values will differ.

Device characteristics

Capacity (native)	536,870,912 byte (536MB)
Max LBA (native)	1,048,575 (0FFFFFh)
Required size for protected area	8,388,608 byte
Required blocks for protected area	16,384 (004000h)
Customer usable device size	528,482,304 byte (528MB)
Customer usable sector count	1,032,192 (0FC000h)
LBA range for protected area	0FC000h to 0FFFFFh

1. Shipping HDDs from the HDD manufacturer

   When the HDD is shipped from the manufacturer, the device has been tested to have a capacity of 536 MB, flagging the media defects not visible by the system.

2. Preparing HDDs at system manufacturer

   Special utility software is required to define the size of the protected area and store the data in it. The sequence is:

   Issue Read Native Max ADDRESS command to get the real device max. of LBA/CYL. Returned value shows that native device Max LBA is 0FFFFFh regardless of the current setting.

   Make entire device accessible, including the protected area, by setting the device Max LBA as

   0FFFFFh via Set Max ADDRESS command. The option could be either nonvolatile or volatile.

Test the sectors for protected area (LBA > = 0FC000h) if required.

Write information data such as BIOS code within the protected area.

Change maximum LBA using Set Max ADDRESS command to 0FBFFFh with nonvolatile option.

From this point, the protected area cannot be accessed until next Set Max ADDRESS command is issued. Any BIOS, device driver, or application software accesses the HDD as if it is a 528 MB device because the device behaves like a 528 MB device.

3. Conventional usage without system software support:
   Since the HDD works as a 528 MB device, there is no special care required for normal use of this device.

4. Advanced usage using protected area:
   The data in the protected area is accessed by the following steps.

   Issue Read Native Max ADDRESS command to get the real device max.

   LBA/CYL. Returned value shows that native device Max LBA is 0FFFFFh regardless of the current setting.

   Make entire device accessible, including the protected area, by setting device Max LBA as 0FFFFFh via Set Max ADDRESS command with the volatile option. By using this option, unexpected power removal or reset will prevent the protected area from remaining accessible.

   Read information data from protected area.

   Issue hard reset or POR to inhibit any access to the protected area.

11.9.2 Set Max security extension commands

The Set Max SET PASSWORD command allows the host to define the password to be used during the current power on cycle. This password is not related to the password used for the Security Mode Feature set. When the password is set the device is in the Set Max Unlocked mode.

This command requests a transfer of a single sector of data from the host. The following figure defines the content of this sector of information. The password is retained by the device until the next power cycle. When the device accepts this command the device is in Set Max Unlocked mode.

Word	Content
0	Reserved
1-16	Password (32 bytes)
17-255	Reserved

Figure 65. Set Max SET PASSWORD data content

The Set Max LOCK command allows the host to disable the Set Max commands (except Set Max UNLOCK and Set Max FREEZE LOCK) until the next power cycle or the issuance and acceptance of the Set Max UNLOCK command. When this command is accepted the device is in the Set Max Locked mode.

The Set Max UNLOCK command changes the device from the Set Max Locked mode to the Set Max Unlocked mode.

This command requests a transfer of a single sector of data from the host. The figure shown above defines the content of this sector of information. The password supplied in the sector of data transferred is compared with the stored Set Max password. If the password compare fails, then the device returns command aborted and decrements the unlock counter. On the acceptance of the Set Max LOCK command, this counter is set to a value of five and is decremented for each password mismatch when Set Max UNLOCK is issued and the device is locked. When this counter reaches zero, then the Set Max UNLOCK command returns command aborted until a power cycle.

The Set Max FREEZE LOCK command allows the host to disable the SET MAX commands (including Set Max UNLOCK) until the next power cycle. When this command is accepted the device is in the Set Max Frozen mode.

The Set Max password, the Set Max security mode and the unlock counter don't persist over a power cycle but persist over a hardware or software reset.

NOTE: If this command is immediately preceded by a Read Native MAX ADDRESS command regardless of Feature register value, it shall be interpreted as a Set Max ADDRESS command.

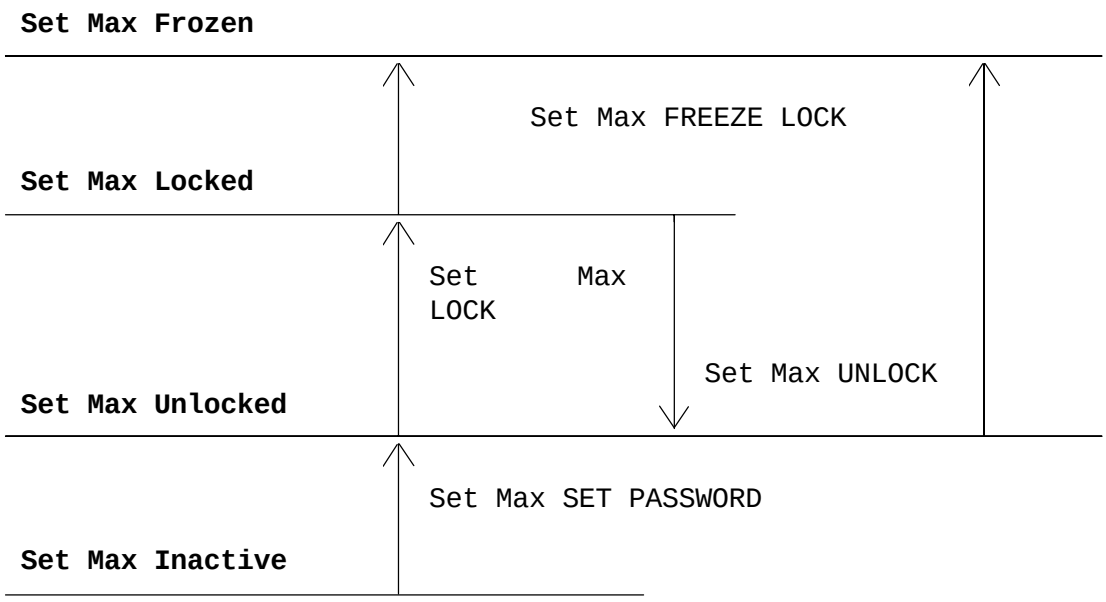

Figure 66. Set Max security mode transition

11.10 Address Offset Feature (vendor specific)

Computer systems perform initial code loading (booting) by reading from a predefined address on a disk drive. To allow an alternate bootable operating system to exist in a reserved area on a disk drive this feature provides a Set Features function to temporarily offset the drive address space. The offset address space wraps around so that the entire disk drive address space remains addressable in offset mode. The Set Max pointer is set to the end of the reserved area to protect the data in the user area when operating in offset mode. This protection can be removed by a Set Max Address command to move the Set Max pointer to the end of the drive. But any commands which access sectors across the original native maximum LBA are rejected with error, even if this protection is removed by a Set Max Address command.

11.10.1 Enable/Disable Address Offset Mode

Subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, LBA 0, to the start of the nonvolatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by the Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a nonvolatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command the command fails with Abort error status.

Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last nonvolatile Set Max Address command.

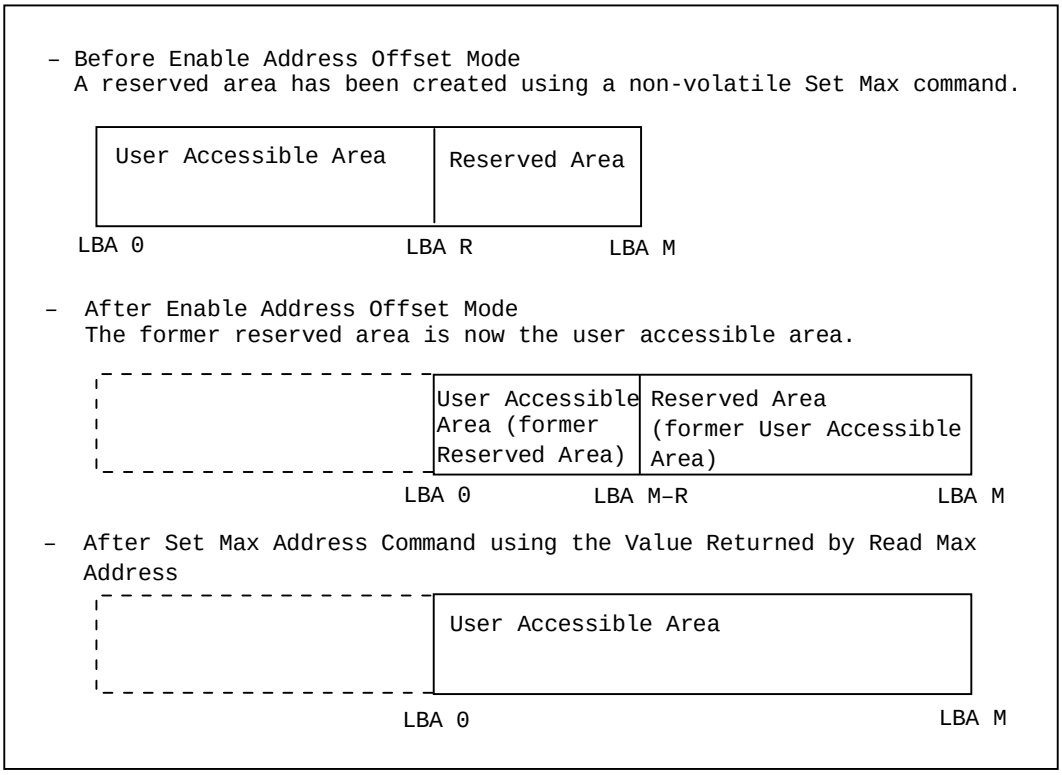

Figure 67. Device address map before and after Set Feature

11.10.2 Identify Device Data

Identify Device data, word 83, bit 7 indicates the device supports the Address Offset Feature. Identify Device data, word 86, bit 7 indicates the device is in Address Offset mode.

11.10.3 Exceptions in Address Offset Mode

Any commands which access sectors across the original native maximum LBA are rejected with error, even if the access protection is removed by a Set Max Address command.

Read Look Ahead operation is not carried out, even if it is enabled by the Set Feature command.

11.11 Seek Overlap

DJSA-XXX drives provide accurate seek time measurement method. The seek command is usualy used to measure the device seek time by accumulating execution time for a number of seek commands. With typical implementation of the seek command, this measurement must include the device and host command overhead. To eliminate this overhead, the DJSA-XXX drive overlaps the seek command as described below.

The first seek command completes before the actual seek operation is over. Then the device can receive the next seek command from the host. However, actual seek operation for the next seek command starts right after completion of the actual seek operation for the first seek command. The execution of two seek commands overlaps excluding the actual seek operation.

With this overlap, total elapsed time for a number of seek commands is the total accumulated time for the actual seek operation plus one pre and post overhead. When the number of seeks is large, this overhead can be ignored.

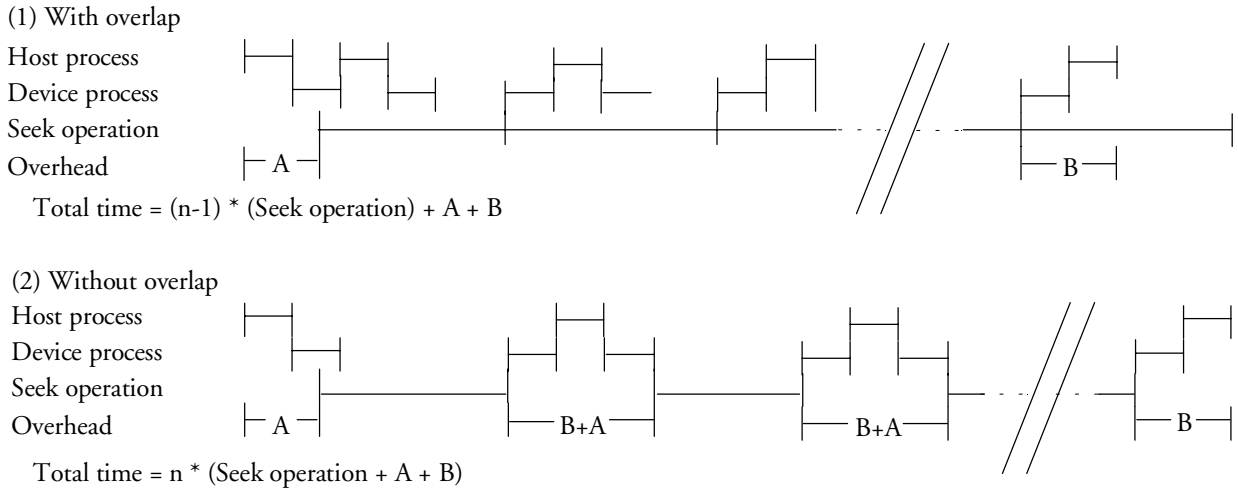

Figure 68. Seek overlap

11.12 Write Cache function

Write cache is a performance enhancement whereby the device reports completion of the write command (Write Sectors and Write Multiple) to the host as soon as the device has received all of the data in its buffer. The device assumes responsibility to write the data subsequently onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation, but power off terminates writing operation immediately and unwritten data is lost.
- Flush cache, Soft reset, Standby, Standby Immediate and Sleep are executed after the completion of writing to disk media on enabling write cache function. The host system can confirm the completion of write cache operation by issuing flush cache command, Soft reset, Standby command, Standby Immediate command or Sleep command, and confirming the completion of the issued command.
- The retry bit of Write Sectors is ignored when write cache is enabled.

11.13 Delayed Write function (vendor specific)

Delayed Write function is a power saving enhancement whereby the device delays the actual data writing into the media. When the device is in the power saving mode and the Write command (Write Sectors, Write Multiple, or Write DMA) comes from the host, the transferred data is not written into the media immediately, only stored into the cache buffer. When the cache buffer becomes full or reaches the predefined size, or if any command except the Write command is issued, the operation to write the data from the cache buffer into the media is begun.

Power consumption can be reduced by Delayed Write. When Write commands come with a long interval, the device must exit from the power saving mode and enter into the power saving mode again without Delayed Write function. If Delayed Write is enabled, such power saving mode transition times can be reduced. As a result, the additional energy for power saving mode transition can be saved, then the average power consumption of the device can be reduced.

However, the time elapsed from the completion of the Write command to the media write completion will be extended with Delayed Write function. If the power for the device is turned off during this time, the data which has not been written to the media is lost. Therefore, a command listed in the Write Cache Function section shall be issued before the power off to confirm whole cached data has been written into the media.

For safety, Delayed Write function is disabled at Power On Default. The Enable Delayed Write command is issued to the device to enable Delayed Write function every Power On Reset or Hard Reset. The actions of each reset are shown in Figure 54 on page 72.

11.13.1 Enable/Disable Delayed Write command

Command code FAh with Feature register 07h enables Delayed Write function.

Command code FAh with Feature register 87h disables Delayed Write function.

Ensure that even if Delayed Write function is enabled by this command, Delayed Write does not work when Write Cache function is disabled.

11.14 Reassign Function

The Reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector. The one entry can register 256 consecutive sectors maximum.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the reassign function will be disabled automatically.

The spare sectors for reassignment are located in a reserved area. As a result of reassignment, the physical location of logically sequenced sectors is dispersed.

11.14.1 Auto Reassign Function

The sectors that show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located in a reserved area. The conditions for auto-reallocation are described below.

Nonrecovered write errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation fails.

If the number of available spare sectors reaches 16 sectors, the write cache function will be disabled automatically.

If the command is without retry and the write cache function is disabled, the auto reassign function is not invoked.

Nonrecovered read errors

When a read operation fails after a defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verifications is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector failed once and then recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the predefined conditions.

12.0 Command protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check to see if BSY = 1, and should proceed no further unless and until BSY = 0. For all commands, the host must also wait for RDY = 1 before proceeding.

A device must maintain either BSY = 1 or DRQ = 1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY = 1 or DRQ = 1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 128 on page 187 shows the device time-out values.

12.1 Data In commands

These commands are:

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors
- S.M.A.R.T. Read Attribute Values
- S.M.A.R.T. Read Attribute Thresholds
- S.M.A.R.T. Read log sector

Execution includes the transfer of one or more 512 byte (> 512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
   a. The device sets BSY = 1 and prepares for data transfer.
   b. When a sector (or block) of data is available for transfer to the host, the device sets BSY = 0, sets DRQ = 1, and interrupts the host.
   c. In response to the interrupt, the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads one sector (or block) of data via the Data Register.

f. The device sets DRQ = 0 after the sector (or block) has been transferred to the host.

4. For the Read Long command:

   a. The device sets BSY = 1 and prepares for data transfer.

   b. When the sector of data is available for transfer to the host, the device sets BSY = 0, sets DRQ = 1, and interrupts the host.

   c. In response to the interrupt, the host reads the Status Register.

   d. The device clears the interrupt in response to the Status Register being read.

   e. The host reads the sector of data including ECC bytes via the Data Register.

   f. The device sets DRQ = 0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register before the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY = 0, ERR = 1, ABT = 1, and interrupting the host.

If an error occurs, the device will set BSY = 0, ERR = 1, and DRQ = 1. The device will then store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The error location will be reported using CHS mode or LBA mode. The mode is decided by the mode select bit (bit 6) of the Device/Head register upon issuing the command.

If an Uncorrectable Data Error (UNC = 1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available for transfer to the host, at the host's option. In case of a Read Multiple command, the host should complete transfer of the block which includes the error from the sector buffer and terminate whatever the error type that occurred.

If an error occurs that is correctable using retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits. The ECC bytes are an exception having only 8 bits.

12.2 Data Out commands

The following are examples of Data Out commands:

- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Set Max SET PASSWORD
- Set Max UNLOCK
- S.M.A.R.T. Write log sector
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors
- Write Verify

Execution includes the transfer of one or more 512 byte (> 512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY = 1.
4. For each sector (or block) of data to be transferred:
   a. The device sets BSY = 0 and DRQ = 1 when it is ready to receive a sector (or block).
   b. The host writes one sector (or block) of data via the Data Register.
   c. The device sets BSY = 1 after it has received the sector (or block).
   d. When the device has finished processing the sector (or block), it sets BSY = 0, and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
   a. The device sets BSY = 0 and DRQ = 1 when it is ready to receive a sector.
   b. The host writes one sector of data including ECC bytes via the Data Register.
   c. The device sets BSY = 1 after it has received the sector.
   d. After processing the sector of data the device sets BSY = 0 and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, then it will abort the command by setting BSY = 0, ERR = 1, ABT = 1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY = 0 and ERR = 1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The error location will be reported with CHS mode or LBA mode. The mode is decided by the mode select bit (bit 6) of the Device/Head register on issuing the command.

All data transfers to the host through the Data Register are 16 bits. The ECC bytes are an exception having only 8 bits.

12.3 Nondata commands

The following are examples of Nondata commands:

- Check Power Mode
- Enable/Disable Delayed Write
- Execute Device Diagnostic
- Flush Cache
- Format Unit
- Idle
- Idle Immediate

- Initialize Device Parameters
- Read Native Max ADDRESS
- Read Verify Sectors
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Sense Condition
- Set Features
- Set Max ADDRESS
- Set Max LOCK
- Set Max FREEZE LOCK
- Set Multiple Mode
- Sleep
- S.M.A.R.T. Disable Operations
- S.M.A.R.T. Enable/Disable Attribute Auto sav
- S.M.A.R.T. Enable/Disable Automatic Off-line
- S.M.A.R.T. Enable Operations
- S.M.A.R.T. Execute Off-line Immediate
- S.M.A.R.T. Return Status
- S.M.A.R.T. Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY = 1.
4. When the device has finished processing the command, it sets BSY = 0 and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The device clears the interrupt in response to the Status Register being read.

12.4 DMA Data Transfer commands

These commands are:

- Identify Device DMA
- Read DMA
- Write DMA

Data transfers using DMA commands differ in two ways from PIO transfers:

- Data transfers are performed using the Slave DMA channel
- No intermediate sector interrupts are issued on multisector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands. The difference is that the host does not initializes the Slave DMA channel prior to issuing the command.

The interrupt handler for DMA transfers differs as follows:

- No intermediate sector interrupts are issued on multisector commands.
- The host resets the DMA channel prior to reading status from the device.

The DMA protocol allows high performance multitasking operating systems to eliminate processor overhead associated with PIO transfers.

1. The host initializes the Slave DMA channel.
2. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
3. The host writes command code to the Command Register.
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. The host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. The host resets the Slave DMA channel.
8. The host reads the Status Register and, optionally, the Error Register.

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13.0 Command descriptions

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
3	Check Power Mode	E5	1 1 1 0 0 1 0 1
3	Check Power Mode*	98	1 0 0 1 1 0 0 0
3	Enable/Disable Delayed Write	FA	1 1 1 1 1 0 1 0
3	Execute Device Diagnostic	90	1 0 0 1 0 0 0 0
3	Flush Cache	E7	1 1 1 0 0 1 1 1
2	Format Track	50	0 1 0 1 0 0 0 0
3	Format Unit	F7	1 1 1 1 0 1 1 1
1	Identify Device	EC	1 1 1 0 1 1 0 0
4	Identify Device DMA	EE	1 1 1 0 1 1 1 0
3	Idle	E3	1 1 1 0 0 0 1 1
3	Idle*	97	1 0 0 1 0 1 1 1
3	Idle Immediate	E1	1 1 1 0 0 0 0 1
3	Idle Immediate*	95	1 0 0 1 0 1 0 1
3	Initialize Device Parameters	91	1 0 0 1 0 0 0 1
1	Read Buffer	E4	1 1 1 0 0 1 0 0
4	Read DMA (retry)	C8	1 1 0 0 1 0 0 0
4	Read DMA (no retry)	C9	1 1 0 0 1 0 0 1
3	NOP	00	0 0 0 0 0 0 0 0
1	Read Buffer	E4	1 1 1 0 0 1 0 0
0	Read Long (retry)	22	0 0 1 0 0 0 1 0
1	Read Long (no retry)	23	0 0 1 0 0 0 1 1
1	Read Multiple	C4	1 1 0 0 0 1 0 0
3	Read Native Max ADDRESS	F8	1 1 1 1 1 0 0 0
1	Read Sectors (retry)	20	0 0 1 0 0 0 0 0
1	Read Sectors (no retry)	21	0 0 1 0 0 0 0 1
3	Read Verify Sectors (retry)	40	0 1 0 0 0 0 0 0
3	Read Verify Sectors (no retry)	41	0 1 0 0 0 0 0 1
3	Recalibrate	1x	0 0 0 1 – – – –
2	Security Disable Password	F6	1 1 1 1 1 0 1 0
3	Security Erase Prepare	F3	1 1 1 1 0 0 1 1
2	Security Erase Unit	F4	1 1 1 1 0 1 0 0
3	Security Freeze Lock	F5	1 1 1 1 0 1 0 1
2	Security Set Password	F1	1 1 1 1 0 0 0 1
2	Security Unlock	F2	1 1 1 1 0 0 1 0
3	Seek	7x	0 1 1 1 – – – –
3	Sense Condition	F0	1 1 1 1 0 0 0 0
3	Set Features	EF	1 1 1 0 1 1 1 1
3	Set Max ADDRESS	F9	1 1 1 1 1 0 0 1
3	Set Max FREEZE LOCK	F9	1 1 1 1 1 0 0 1
3	Set Max LOCK	F9	1 1 1 1 1 0 0 1
2	Set Max SET PASSWORD	F9	1 1 1 1 1 0 0 1

Figure 69. Command set (1 of 2)

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
2	Set Max UNLOCK	F9	1 1 1 1 1 0 0 1
3	Set Multiple Mode	C6	1 1 0 0 0 1 1 0
3	Sleep	E6	1 1 1 0 0 1 1 0
3	Sleep*	99	1 0 0 1 1 0 0 1
3	S.M.A.R.T. Disable Operations	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Enable/Disable Attribute Auto save	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Enable/Disable Automatic Off-line	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Enable Operations	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Execute Off–line Immediate	B0	1 0 1 1 0 0 0 0
1	S.M.A.R.T. Read Attribute Values	B0	1 0 1 1 0 0 0 0
1	S.M.A.R.T. Read Attribute Thresholds	B0	1 0 1 1 0 0 0 0
1	S.M.A.R.T. Read Log Sector	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Return Status	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Save Attribute Values	B0	1 0 1 1 0 0 0 0
2	S.M.A.R.T. Write Log Sector	B0	1 0 1 1 0 0 0 0
3	Standby	E2	1 1 1 0 0 0 1 0
3	Standby*	96	1 0 0 1 0 1 1 0
3	Standby Immediate	E0	1 1 1 0 0 0 0 0
3	Standby Immediate*	94	1 0 0 1 0 1 0 0
2	Write Buffer	E8	1 1 1 0 1 0 0 0
4	Write DMA (retry)	CA	1 1 0 0 1 0 1 0
4	Write DMA (no retry)	CB	1 1 0 0 1 0 1 1
2	Write Long (retry)	32	0 0 1 1 0 0 1 0
2	Write Long (no retry)	33	0 0 1 1 0 0 1 1
2	Write Multiple	C5	1 1 0 0 0 1 0 1
2	Write Sectors (retry)	30	0 0 1 1 0 0 0 0
2	Write Sectors (no retry)	31	0 0 1 1 0 0 0 1
2	Write Verify	3C	0 0 1 1 1 1 0 0

Protocol: 1 : PIO data IN command
2 : PIO data OUT command
3 : Non data command
4 : DMA command

Commands marked * are alternate command codes for previously defined commands.

Figure 69. Command set (2 of 2)

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
(Delayed Write Function)		
Enable Delayed Write function	FA	07
Disable Delayed Write function	FA	87
(S.M.A.R.T Function)		
S.M.A.R.T. Read Attribute Values	B0	D0
S.M.A.R.T. Read Attribute Thresholds	B0	D1
S.M.A.R.T. Enable/Disable Attribute Autosave	B0	D2
S.M.A.R.T. Save Attribute Values	B0	D3
S.M.A.R.T. Execute Off–line Immediate	B0	D4
S.M.A.R.T. Read Log Sector	B0	D5
S.M.A.R.T. Write Log Sector	B0	D6
S.M.A.R.T. Enable Operations	B0	D8
S.M.A.R.T. Disable Operations	B0	D9
S.M.A.R.T. Return Status	B0	DA
S.M.A.R.T. Enable/Disable Automatic Off-line	B0	DB
(Set Features)		
Enable Write Cache	EF	02
Set Transfer mode	EF	03
Enable Advanced Power Management feature	EF	05
Enable Address Offset mode	EF	09
40 bytes of ECC apply on Read/Write Long	EF	44
Disable read look–ahead feature	EF	55
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Disable Advanced Power Management feature	EF	85
Disable Address Offset mode	EF	89
Enable read look–ahead feature	EF	AA
4 bytes of ECC apply on Read/Write Long	EF	BB
Enable reverting to power on defaults	EF	CC
(Set Max Security Extension)		
Set Max SET PASSWORD	F9	01
Set Max LOCK	F9	02
Set Max UNLOCK	F9	03
Set Max FREEZE LOCK	F9	04

Figure 70. Command Set (Subcommand)

Figure 68 on pages 103 and 104 shows the commands that are supported by the device.

Figure 69 above shows the subcommands that are supported by each command or feature.

The following symbols are used in the command descriptions:

Output Registers

0 This indicates that the bit must be set to 0.

1 This indicates that the bit must be set to 1.

D The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.

H Head number. This indicates that the head number part of the Device/Head Register is an output parameter and should be specified.

L LBA mode. This indicates the addressing mode. Zero specifies CHS mode and one specifies LBA addressing mode.

R Retry. This indicates that the Retry bit of the Command Register be specified.

B Option Bit. This indicates that the Option Bit of the Sector Count Register be specified. (This bit is used by Set Max ADDRESS command.)

V Valid. This indicates that the bit is part of an output parameter and should be specified.

x This indicates that the hex character is not used.

- This indicates that the bit is not used.

Input Registers

0 This indicates that the bit is always set to 0.

1 This indicates that the bit is always set to 1.

H Head number. This indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.

V Valid. This indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.

N Not recommendable condition for start up. Indicates that the condition of device is not recommendable for start up.

- This indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

13.1 Check Power Mode (E5h/98h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	V V V V V V V V
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 1 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 71. Check Power Mode command (E5h/98h)

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count This indicates the power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register is set to 0.

13.2 Enable/Disable Delayed Write (FAh: vendor specific)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	V V V V V V V V		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 1 0 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	–	–	0	–	V

Figure 72. Enable/Disable Delayed Write command (FAh)

The Enable/Disable Delayed Write command sets if the Delayed Write function is enabled or disabled. Delayed Write function is enabled or disabled according to the feature register's value.

Even if the Delayed Write function is enabled by this command, Delayed Write does not work when the Write Cache function is disabled.

For details for this function, refer to section 11.13, "Delayed Write Function (Vendor Specific)" on page 95.

Output Parameters To The Device

Feature This is the destination code for this command.

07H is the Enable Delayed Write function

87H is the Disable Delayed Write function

13.3 Execute Device Diagnostic (90h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 – – – – –		Device/Head	– – – – – – – –
Command	1 0 0 1 0 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	–	–	0	–	0

Figure 73. Execute Device Diagnostic command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 56 on page 73 for the definition.

13.4 Flush Cache (E7h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 1 1 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 74. Flush Cache command (E7h)

This command causes the device to complete writing data from its cache.

The device returns a status of RDY = 1 and DSC = 1 (50h) after following sequence.

- Data in the write cache buffer is written to the disk media.
- There is a return of a successful write completion to the disk media.

13.5 Format Track (50h: vendor specific)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	0 1 0 1 0 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 75. Format Track command (50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with the write operation. At this time, the read operation is not verified for the correct sector of data initialization. Any data previously stored on the track will be lost.

The host transfers a sector of data containing a format table to the device. The format table should contain two bytes for each sector on the track to be formatted. The structure of the format table is shown in Figure 75 on page 112. The first byte should contain a descriptor value and the second byte should contain the sector number. The descriptor value should be 0 for a good sector. Any other descriptor value will cause an aborted error. The remaining bytes of the sector following the format table are ignored.

Since device performance is optimal at a 1:1 interleave, and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Device

Sector Number In LBA mode this register specifies that LBA address bits 0–7 are to be formatted. (L = 1)

Cylinder High/Low This indicates the cylinder number of the track to be formatted. (L = 0)

In LBA mode this register specifies that LBA address bits 8–15 (Low) and bits 16–23 (High) are to be formatted. (L = 1)

H This indicates the head number of the track to be formatted. (L = 0)

In LBA mode this register specifies that LBA address bits 24–27 are to be formatted. (L = 1)

Input Parameters From The Device

Sector Number In LBA mode this register specifies the current LBA address bits as 0–7 (L = 1).

Cylinder High/Low In LBA mode this register specifies the current LBA address bits as 8–15 (Low) and bits 16–23 (High).

H In LBA mode this register specifies the current LBA address bits as 24–27 (L = 1).

Error This indicates the Error Register. An Abort error (ABT = 1) will be returned under the following conditions:

- The descriptor value does not match the certain value (except 00h).

In LBA mode this command formats a single logical track including the specified LBA.

Explanation for descriptor

Descriptor : 00h This indicates the sector of data will be initialized to 00h.

Byte	Data	Description
0 1	xxh 00h	descriptor value for sector number 00h sector number
2 3	xxh 01h	descriptor value for sector number 01h sector number
4 5	xxh 02h	descriptor value for sector number 02h sector number
: :	: :	
N*2 N*2+1	xxh N	descriptor value for sector number N sector number (last sector for the track)
N*2+2 N*2+3 : : 510 511	00h 00h : : 00h 00h	remainder of buffer filled with 00h

Descriptor : 00h—Format sector as good sector

Figure 76. Format track data field format

13.6 Format Unit (F7h: vendor specific)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	V V V V V V V V		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 1 1 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 77. Format Unit command (F7h)

The Format Unit command initializes all user data sectors after merging the reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available right after this command's completion. This commands completion is also used on the next power on reset or hard reset. Both previous information data are erased from the device by this command.

Note that the Format Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA is set by Initialize Drive Parameter or Set MAX ADDRESS command is ignored. The protected area by Set MAX ADDRESS command is also initialized.

The Security Erase Prepare command should be completed immediately prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command the device aborts the Format Unit command.

If the Feature register is NOT 11h, the device returns an Abort error to the host.

This command does not request to do a data transfer.

Output Parameters To The Device

Feature This indicates the Destination code for this command.

11H The merge reassigned location into the defect information.

The execution time of this command is shown below.

DJSA-232	about 39 minutes
DJSA-230	about 42 minutes
DJSA-220	about 30 minutes
DJSA-210	about 16 minutes
DJSA-205	about 8 minutes

13.7 Identify Device (ECh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 1 1 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 78. Identify Device command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Figure 78 on pages 115–121.

Word	Content		Description	
00	045AH		Drive classification	Bit assignments
			15(=0)	1=ATAPI device, 0=ATA device
		*	14(=0)	1=format speed tolerance gap required
		*	13(=0)	1=track offset option available
		*	12(=0)	1=data strobe offset option available
		*	11(=0)	1=rotational speed tolerance > 0.5%
		*	10(=1)	1=disk transfer rate > 10 Mbps
		*	9(=0)	1=disk transfer rate > 5 Mbps but <= 10 Mbps
		*	8(=0)	1=disk transfer rate <= 5 Mbps
			7(=0)	1=removable cartridge drive
			6(=1)	1=fixed drive
		*	5(=0)	1=spindle motor control option implemented
		*	4(=1)	1=head switch time > 15 us
		*	3(=1)	1=not MFM encoded
			2(=0)	1=identify data incomplete
		*	1(=1)	1=hard sectored
			0(=0)	Reserved
01	Note1		Number of cylinders in default translate mode	
02	C837H		SET FEATURES subcommand is not required to spin-up and IDENTIFY DEVICE response is complete	
03	Note1		Number of heads in default translate mode	
04	0	*	Reserved	
05	0	*	Reserved	
06	003FH		Number of sectors per track in default translate mode	
07	0		Reserved	
08	0		Reserved	
09	0000H	*	Reserved	
10–19	XXXX		Serial number in ASCII (0 = not specified)	
20	0003H	*	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read	
21	Note1	*	Buffer size in 512-byte increments	
22	00XXH	*	Number of ECC bytes as currently selected via the set feature command	
23–26	XXXX		Micro code version in ASCII	
27–46	Note1		Model number in ASCII	
47	8010H		Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands 15–8(=80h) 7–0 : Maximum number of sectors that can be transferred per interrupt.	

*Note. The ' *' mark in the 'Content' field indicates the use of those parameters that are vendor specific.*
Note1. See the Figure 79.

Figure 79. Identify device information (1 of 7)

Word	Content		Description
48	0000H	*	Capable of double word I/O, '0000'= cannot perform
49	0F00H		Capabilities, bit assignments: 15-14(=0) Reserved 13(=0) Standby timer value are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) Reserved 8(=0) Reserved
		*	7–0(=0) Reserved
50	0000H		Capabilities 15(=0) 0=the contents of word 50 are valid 14(=1) 1=the contents of word 50 are valid 13– 1(=0) Reserved 0(=0) 1=the device has a minimum Standby timer value that is device specific
51	0200H		PIO data transfer cycle timing mode
52	0200H	*	DMA data transfer cycle timing mode Refer Word 62 and 63
53	XXX7H		Validity flag of the word 15– 3(=0) Reserved 2(=1) 1=Word 88 is Valid 1(=1) 1=Word 64–70 are Valid 0(=1) 1=Word 54–58 are Valid
54	XXXXH		Number of current cylinders
55	XXXXH		Number of current heads
56	XXXXH		Number of current sectors per track
57–58	XXXXH		Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH		Current Multiple setting. Bit assignments: 15– 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7– 0 xxh = Current setting for number of sectors
60–61	Note1		Total Number of User Addressable Sectors Word 60 specifies the low word of the number
62	0000H	*	Reserved
63	XX07H		Multiword DMA Transfer Capability 15–11(=0) Reserved 10 1=Multiword DMA mode 2 is selected 9 1=Multiword DMA mode 1 is selected 8 1=Multiword DMA mode 0 is selected 7– 0(=7) Multiword DMA transfer modes supported (support mode 0, 1 and 2)

*Note. The ' *' mark in the 'Content' field indicates the use of those parameters that are vendor specific.*
Note1. See Figure 79.

Figure 79. Identify device information (2 of 7)

Word	Content	Description
64	0003H	Flow Control PIO Transfer Modes Supported 15– 8(=0) Reserved 7– 0(=3) Advanced PIO Transfer Modes Supported ‘11’ = PIO Mode 3 and 4 Supported
64	0003H	Flow Control PIO Transfer Modes Supported 15– 8(=0) Reserved 7– 0(=3) Advanced PIO Transfer Modes Supported ‘11’ = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15–0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
66	0078H	Manufacturer’s Recommended Multiword DMA Transfer Cycle Time 15– 0(=78) Cycle time in nanoseconds(120ns, 16.6MB/s)
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15– 0(=F0) Cycle time in nanoseconds (240ns, 8.3MB/s)
68	0078H	Minimum PIO Transfer Cycle Time WithIORDY Flow Control 15– 0(=78) Cycle time in nanoseconds (120ns,16.6MB/s)
69–79	0000H	Reserved
80	003CH	Major version number ATA-1, ATA-2, ATA-3 and ATA/ATAPI-4, ATA/ATAPI-5
81	0015H	Minor version number ATA/ATAPI-5 T13 1321D Revision 1
82	746BH	Command set supported 15(=0) Reserved 14(=1) 1=NOP command supported 13(=1) 1=READ BUFFER command supported 12(=1) 1=WRITE BUFFER command supported 11(=0) Reserved 10(=1) 1=Host Protected Area Feature Set Supported 9(=0) 1=DEVICE RESET command supported 8(=0) 1=SERVICE interrupt supported 7(=0) 1=release interrupt supported 6(=1) 1=look-ahead supported 5(=1) 1=write cache supported 4(=0) 1=supported PACKET Command Feature Set 3(=1) 1=supported Power Management Feature Set 2(=0) 1=supported Removable Media Feature Set 1(=1) 1=supported Security Feature Set 0(=1) 1=supported S.M.A.R.T. Feature Set

Figure 79. Identify device information (3 of 7)

Word	Content	Description
83	41A8H	Command set supported 15(=0) Always 14(=1) Always 13– 9(=0) Reserved 8(=1) 1=SET MAX security extension supported 7(=1) 1=Address Offset feature supported 6(=0) 1=SET FEATURES subcommand required to spin-up 5(=1) 1=Power-Up In Standby feature set supported 4(=0) 1=Removable Media Status Notification Feature Set supported 3(=1) 1=Advanced Power Management Feature Set supported 2(=0) 1=CPA Feature Set supported 1(=0) 1=READ/WRITE DMA QUEUED supported 0(=0) 1=DOWNLOAD MICROCODE command supported
84	4000H	Command set/feature supported extension 15(=0) Always 14(=1) Always 13– 0(=0) Reserved
85	F4XXH	Command set/feature enabled 15(=1) Reserved 14(=1) 1=NOP command supported 13(=1) 1=READ BUFFER command supported 12(=1) 1=WRITE BUFFER command supported 11(=0) Reserved 10(=1) 1=Host Protected Area Feature Set supported 9(=0) 1=DEVICE RESET command supported 8(=0) 1=SERVICE interrupt enabled 7(=0) 1=release interrupt enabled 6(=X) 1=look-ahead enabled 5(=X) 1=srite cache enabled 4(=0) 1=supports PACKET Command Feature Set 3(=X) 1=supports Power Management Feature Set 2(=0) 1=supports Removable Media Feature Set 1(=X) 1=Security Feature Set enabled 0(=X) 1=S.M.A.R.T. Feature Set enabled

Figure 79. Identify device information (4 of 7)

Word	Content	Description
86	00XXH * *	Command set/feature enabled 15– 8(=0) Reserved 7(=X) 1=Address Offset mode enabled 6(=0) 1=SET FEATURES subcommand required to spin-up 5(=0) 1=Power-Up In Standby feature set has been enabled via the SET FEATURES command 4(=0) 1=Removable Media Status Notification Feature Set enabled 3(=X) 1=Advanced Power management Feature Set enabled 2(=0) 1=CFA Feature Set supported 1(=0) 1=READ/WRITE DMA QUEUED command supported 0(=0) 1=DOWNLOAD MICROCODE command supported
87	4000H	Command set/feature enabled 15(=0) Always 14(=1) Always 13– 0(=0) Reserved
88	XX1FH	Ultra DMA Transfer mode (mode 4 supported) 15–13(=0) Reserved 12(=X) 1=UltraDMA mode 4 is selected 11(=X) 1=UltraDMA mode 3 is selected 10(=X) 1=UltraDMA mode 2 is selected 9(=X) 1=UltraDMA mode 1 is selected 8(=X) 1=UltraDMA mode 0 is selected 7– 5(=0) Reserved 4(=1) 1=UltraDMA mode 4 is supported 3(=1) 1=UltraDMA mode 3 is supported 2(=1) 1=UltraDMA mode 2 is supported 1(=1) 1=UltraDMA mode 1 is supported 0(=1) 1=UltraDMA mode 0 is supported
89	XXXXH	Time required for security erase unit completion Time= value (XXXXh) * 2 [minutes]
90	0000H	Time required for Enhance security erase completion 0000 : Not supported
91	40XXH	Current Advanced Power Management level 15– 8(=40h) Reserved 7– 0(=X) Correct Advanced Power Management level set by Set Features Command (01h to FEh)
92	XXXXH	Reserved

*Note. The ' *' mark in the 'Content' field indicates the use of those parameters that are vendor specific.*

Figure 79. Identify device information (5 of 7)

Word	Content	Description
93	XXXXH	Hardware reset results Device detected result 15(=0) Reserved 14(=1) Always 13(=X) 1=Device detected CBLID- above V_{iH} 0=Device detected CBLID- below V_{iL} [12- 8 Device 1 hardware reset result Device 0 clear these bits to 0] 12(=0) Reserved 11(=X) 1=Device 1 passed diagnostic 10-9(=X) how Device 1 determined the device number: 00=Reserved 01=a jumper was used 10=the CSEL signal was used 11=some other method was used or the method is unknown 8(=1) Always [7- 0 Device 0 hardware reset result Device 1 clears these bits to 0] 7(=0) Reserved 6(=X) 1=Semi-dupliex mode is enabled 5(=X) 1=Device 0 detected Device 1 4(=X) 1=Device 1 passed diagnostic 3(=X) 1=Device 0 determined the device 2-1(=X) how Device 0 determined the device number: 00=Reserved 01=a jumper was used 10=the CSEL signal was used 11=some other method was used or the method is unknown 0(=1) Always
94-127	0000H	Reserved
128	0XXXH	Security Mode Feature. Bit assignments 15-9(=0) Reserved 8(=X) Security Level 1= Maximum, 0= High 7-6(=0) Reserved 5(=0) 1=Enhanced security erase supported 4(=0) 1=Security count expired 3(=0) 1=Security Frozen 2(=0) 1=Security Locked 1(=0) 1=Security Enable 0(=0) 1=Security Support

Figure 79. Identify device information (6 of 7)

Word	Content	Description
129	000XH	Current Set Feature Option. Bit assignments 15–4(=0) Reserved 3(=X) 1=Auto reassign enabled 2(=X) 1=Reverting enabled 1(=X) 1=Read Look-ahead enabled 0(=X) 1=Write Cache enabled
130	XXXXH *	Reserved
131	000XH *	Initial Power Mode Selection. Bit assignments 15–2(=0) Reserved 1(=1) Always 0(=X) Initial Power Mode 1=Standby, 0=Idle
132–254	0000H *	Reserved
255	XXA5H	Integrity word 15–8(=XX) Checksum 7–0(=A5) Signature

Figure 79. Identify device information (7 of 7)

DJSA-232	
Number of cylinders	3FFFh
Number of heads	10h
Buffer size	0EA5h(=1874 KB)
Model number (ASCII)	IBM-DJSA-232
Total number of user addressable sectors	3B9C460h
DJSA-230	
Number of cylinders	3FFFh
Number of heads	10h
Buffer size	0EA5h(=1874 KB)
Model number (ASCII)	IBM-DJSA-230
Total number of user addressable sectors	37E3E40h
DJSA-220	
Number of cylinders	3FFFh
Number of heads	10h
Buffer size	0EA5h(=1874 KB)
Model number (ASCII)	IBM-DJSA-220
Total number of user addressable sectors	2542980h
DJSA-210	
Number of cylinders	3FFFh
Number of heads	10h
Buffer size	0300h(=384 KB)
Model number (ASCII)	IBM-DJSA-210
Total number of user addressable sectors	12BB230h
DJSA-205	
Number of cylinders	2860h
Number of heads	Fh
Buffer size	0300h(=384 KB)
Model number (ASCII)	IBM-DJSA-205
Total number of user addressable sectors	950A60h

For the microcode revision refer to 13.7, "Identify Device (ECh)"—Figure 77 on page 114—words 23–26. This is 8 characters in ASCII.

Figure 80. Number of cylinders/heads/sectors by models for DJSA-XXX.

13.8 Identify Device DMA (EEh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 1 1 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 81. Identify Device DMA command (EEh)

The Identify Device DMA command requests the device to transfer configuration information to the host. The device will transfer the same 256 words of device identification data by the Identify Device command (ECh) via the DMA channel.

13.9 Idle (E3h/97h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 0 1 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 82. Idle command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately and sets the auto power down time-out Parameter (standby timer). At the set of the auto power down time-out Parameter (standby timer) the point timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and is ready to respond to host commands immediately.

Output Parameters To The Device

Sector Count This indicates the Time-out Parameter. If the time-out Parameter is equal to zero the time-out interval (Standby Timer) is NOT disabled and the time-out interval is set automatically for 109 minutes. If the time-out Parameter is other than zero, the time-out interval is set for (Time-out Parameter × 5) seconds.

The device will enter Standby mode automatically if the time-out interval expires with no device access from the host. The time-out interval will be reinitialized if there is a device access before the time-out interval expires.

13.10 Idle Immediate (E1h/95h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 0 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 83. Idle Immediate command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to the host commands immediately.

The Idle Immediate command will not affect the auto power down time-out parameter.

13.11 Initialize Device Parameters (91h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	– – – – – – – –
Sector Count	V V V V V V V V		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D H H H H		Device/Head	– – – – – – – –
Command	1 0 0 1 0 0 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	–	–	0	–	V

Figure 84. Initialize Device Parameters command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54–58 in Identify Device Information reflects these parameters.

The parameters remain in effect until the following events occur:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- A hard reset occurs.
- A soft reset occurs and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Device

Sector Count This indicates the number of sectors per track. Zero (0) does not mean that there are 256 sectors per track. It means that there are no sectors per track.

H This indicates the number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

13.12 Read Buffer (E4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 1 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 85. Read Buffer command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of the device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

13.13 Read DMA (C8h/C9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	1 1 0 0 1 0 0 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 86. Read DMA command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by the DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that the data transfer has terminated and that status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0) In LBA mode, this register specifies that LBA address bits 0–7 are to be transferred. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0) In LBA mode, this register specifies LBA address bits 8–15 (Low) and 16–23 (High) to be transferred. (L = 1)

H	This indicates the head number of the first sector to be transferred. (L = 0) In LBA mode this register specifies the LBA bits 24–27 to be transferred. (L = 1)
R	This indicates the retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	This indicates the number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	This indicates the sector number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 0–7. (L = 1)
Cylinder High/Low	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the sector to be transferred. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.14 Read Long (22h/23h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	– – – – – – – V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	0 0 1 0 0 0 1 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 87. Read Long command (22h/23h)

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media. It then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 40 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0) In LBA mode, this register contains LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0) In LBA mode, this register contains LBA bits 8–15 (Low), 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0) In LBA mode, this register contains LBA bits 24–27. (L = 1)

R This indicates the retry bit. If it is set to one then retries are disabled.

Input Parameters From The Device

Sector Count This indicates the number of requested sectors not transferred.

Sector Number This indicates the sector number of the transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 8–15 (Low), 16–23 (High). (L = 1)

H This indicates the head number of the transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 24–27. (L = 1)

The device internally uses 40 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. Use of the 40 byte ECC mode is recommended for testing the effectiveness and integrity of the ECC functions of the device.

13.15 Read Multiple (C4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	1 1 0 0 0 1 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 88. Read Multiple command (C4h)

The Read Multiple command reads one or more sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. The command execution is identical to the Read Sectors command with one exception: an interrupt is generated for each block—as defined by the Set Multiple command—instead of for each sector.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified then 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0) In LBA mode, this register contains LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0) In LBA mode this register contains LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0) In LBA mode this register contains LBA bits 24–27. (L = 1)

Input Parameters From The Device

Sector Count	This indicates the number of requested sectors not transferred. This number is zero unless an unrecoverable error occurs.
Sector Number	This indicates the sector number of the last transferred sector. (L = 0) In LBA mode, this register contains the current LBA bits 0–7. (L = 1)
Cylinder High/Low	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode, this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.16 Read Native Max ADDRESS (F8h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	V V V V V V V V
Cylinder Low	– – – – – – – –		Cylinder Low	V V V V V V V V
Cylinder High	– – – – – – – –		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D – – – –		Device/Head	– – – – H H H H
Command	1 1 1 1 1 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 89. Read Native Max ADDRESS (F8h)

This command returns the native max LBA/CYL of HDD which is not effected by the Set Max ADDRESS command. Even if the Address Offset mode is enabled, the native max LBA/CYL of HDD is returned.

Output Parameters To The Device

L LBA mode. This indicates the addressing mode. An L = 0 specifies CHS mode and L = 1 specifies the LBA addressing mode.

D This is the device number bit. Indicates that the device number bit of the Device/Head Register should be specified. D = 0 selects the master device and D = 1 selects the slave device.

- Indicates that the bit is not used.

Input Parameters From The Device

Sector Number In LBA mode this register contains the native max LBA bits 0–7. (L = 1)

In CHS mode this register contains the native max sector number. (L = 0)

Cylinder High/Low In LBA mode this register contains the native max LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

In CHS mode this register contains the native max cylinder number. (L = 0)

H	In LBA mode this register contains the native max LBA bits 24–27. (L = 1) In the CHS mode this register contains the native maximum head number. (L = 0)
V	Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.
-	This indicates that the bit is not used.

13.17 Read Sectors (20h/21h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	0 0 1 0 0 0 0 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 90. Read Sectors command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. If an uncorrectable error occurs the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number This is the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This is the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This is the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This is the retry bit. If is set to one and then retries are disabled.

Input Parameters From The Device

Sector Count	This is the number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	This is the sector number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 0–7. (L = 1)
Cylinder High/Low	This is the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This is the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.18 Read Verify Sectors (40h/41h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	0 0 1 0 0 0 0 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 91. Read Verify Sectors command (40h/41h)

The Read Verify Sectors command verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sectors command and Read Verify Sectors command is: data is transferred to the host during a Read Sectors command; data is not transferred to the host during a Read Verify Sectors command.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

Sector Count This is the number of continuous sectors to be verified. If zero is specified then 256 sectors will be verified.

Sector Number This is the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This is the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H	This is the head number of the first sector to be transferred. (L = 0) In LBA mode this register contains the LBA bits 24–27. (L = 1)
R	This is the retry bit. If it is set to one then retries are disabled.

Input Parameters From The Device

Sector Count	This is the number of requested sectors not verified. This number will be zero unless an unrecoverable error occurs.
Sector Number	This is the sector number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 0–7. (L = 1)
Cylinder High/Low	This is the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This is the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.19 Recalibrate (1xh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	0 0 0 1 – – – –		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 92. Recalibrate command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

13.20 Security Disable Password (F6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 1 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 93. Security Disable Password command (F6h)

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in Figure 93. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be reactivated later by setting User Password. This command should be executed in device unlock mode.

Word	Description
00	Control word bit 0 : Identifier (1–Master, 0–User) bits 1–15 : Reserved
01–16	Password (32 bytes)
17–255	Reserved

Figure 94. Password Information for Security Disable Password command

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

13.21 Security Erase Prepare (F3h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 0 1 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 95. Security Erase Prepare command (F3h)

The Security Erase Prepare command must be issued immediately before the Security Erase Unit command to enable device erasing and unlocking.

The Security Erase Prepare Command must be issued immediately before the Format Unit Command. This command is to prevent accidental erasure of the device.

This command does not request to transfer data.

13.22 Security Erase Unit (F4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 1 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 96. Security Erase Unit command (F4h)

The Security Erase Unit command initializes all user data sectors and then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. The Host MAX LBA is set by the Initialize Drive Parameter or the Set MAX ADDRESS command is ignored. The protected area by the Set MAX ADDRESS command is also initialized.

This command requests the transfer of a single sector of data from the host including information specified in Figure 96.

If the password does not match then the device rejects the command with an Aborted error.

Word	Description
00	Control Word bit 0 : Identifier (1- Master, 0- User) bit 1–15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Figure 97. Erase Unit information

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). After completing of this command, all the user data will be initialized to zero with a write operation. At this time, the data write is not verified with a read operation to determine if the data sector is initialized correctly. At this time the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however, the master password is still stored internally within the device and may be reactivated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the Master Password and the User Password. The device only erases all user data.

The execution time of this command is shown below.

DJSA-232	about 39 minutes
DJSA-230	about 42 minutes
DJSA-220	about 30 minutes
DJSA-210	about 16 minutes
DJSA-205	about 8 minutes

13.23 Security Freeze Lock (F5h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 1 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 98. Security Freeze Lock command (F5h)

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by a Power off.

The following commands are rejected when the device is in frozen mode. Refer to Figure 63 on page 86.

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

13.24 Security Set Password (F1h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 0 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 99. Security Set Password command (F1h)

The Security Set Password command enables the security mode feature (device lock function) and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command and the device is not locked immediately. The device is locked after the next power on reset or hard reset. When the MASTER password is set by this command, the master password is registered internally. The device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in Figure 99 on page 147.

The data transferred controls the function of this command.

Word	Description
00	Control Word bit 0 : Identifier (1- Master, 0- User) bit 1–7 : Reserved bit 8 : Security level (1- Maximum, 0- High) bit 9–15 : Reserved
01–16	Password (32 bytes)
17–18	Master Password Revision Code (valid if Word 0 bit 0 = 1)
19–255	Reserved

Figure 100. Security Set Password information

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

Security Level A zero indicates a High level, a one indicates a Maximum level. If the host sets the High level and the password is forgotten then the Master Password can be used to unlock the device. If the host sets the Maximum level and the user password is forgotten, only an Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

Password The 32 bytes are always significant in the text of the password.

Master Password Revision Code

The Revision Code field is set with Master password. If Identifier is User, the Revision Code is not set. The Revision Code field is returned in the Identify Device word 92. The valid Revision Codes are 0000h to FFFDh. The Default Master Password Revision Code is FFFEh. The code FFFFh is reserved.

The setting of the Identifier and Security level bits interact as follows:

Identifier = User / Security level = High

The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by either the user password or the previously set master password.

Identifier = Master / Security level = High

This combination will set a master password but will NOT enable the security mode feature (lock function).

Identifier = User / Security level = Maximum

The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by only the user password. The master password previously set is still stored in the file but may NOT be used to unlock the device.

Identifier = Master / Security level = Maximum

This combination will set a master password but will NOT enable the security mode feature (lock function).

13.25 Security Unlock (F2h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 1 0 0 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 101. Security Unlock command (F2h)

This command unlocks the password and causes the device to enter device unlock mode. If a power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in Figure 101 on page 150.

If the Identifier bit is set to master and the file is in high security mode then the password supplied will be compared with the stored master password. If the file is in maximum security mode then the security unlock will be rejected.

If the Identifier bit is set to user, then the file compares the supplied password with the stored user password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero, all password protected commands are rejected until there is a hard reset or a power off.

Word	Description
00	Control Word bit 0 : Identifier (1– Master, 0– User) bit 1–15 : Reserved
01–16	Password (32 bytes)
17–255	Reserved

Figure 102. Security Unlock information

Identifier A zero indicates that the device regards Password as the User Password. A one indicates that the device regards Password as the Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password as this is the only reason that an abort error will be returned by the file AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the file then another problem exists.

13.26 Seek (7xh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	0 1 1 1 – – – –		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 103. Seek command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device does not need to be formatted for a seek to execute properly.

Output Parameters To The Device

Sector Number In LBA mode this register specifies the LBA address bits 0–7 for seek. (L = 1)

Cylinder High/Low This is the cylinder number of the seek.

In LBA mode this register specifies the LBA address bits 8–15 (Low) and bits 16–23 (High) for seek. (L = 1)

H This indicates the head number of the seek.

In LBA mode this register specifies the LBA address bits 24–27 for seek. (L = 1)

Input Parameters From The Device

Sector Number In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.27 Sense Condition (F0h: vendor specific)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	0 0 0 0 0 0 0 1		Error	see below
Sector Count	– – – – – – – –		Sector Count	V V V V V V V V
Sector Number	– – – – – – – –		Sector Number	– – – – – – – N
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – D – – – –
Command	1 1 1 1 0 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	V	–	V	–	–	V

Figure 104. Sense Condition Command (F0h)

The Sense Condition command is used to sense temparature in a device.This command is executable winthout spinning up even if a device is started with No Spin Up option.

Output Parameters To The Device

Feature The Feature register must be set to 01h. All other value are rejected with setting ABORT bit in status register.

Input Parameters From The Device

Sector Count The Sector Count register contains result value.

Value	Description
00h	Temperature is equal to or lower than –20°C
01h–FEh	Temperature is (Value/2–20)°C
FFh	Temperature is higher than 107°C

N Not recommendable condition for start up. If over stressed condition is detected, this bit will be set to one.

13.28 Set Features (EFh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	V V V V V V V V		Error	see below
Sector Count	*Note 1.*		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 1 1 1 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 105. Set Features command (EFh)

The Set Feature command establishes the following parameters which affect the execution of certain features as shown in the table below.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

After the power on reset or hard reset the device is set to the following features as default.

```
Write cache                                : Enable
ECC bytes                                  : 4 bytes
Read look-ahead                            : Enable
Reverting to power on defaults             : Disable
Address Offset mode                        : Disable
```

Output Parameters To The Device

Feature Destination code for this command.

02H Enable write cache (See note 2)

03H Set transfer mode based on value in sector count register

05H Enable Advanced Power Management

09H Enable Address Offset mode

44H 40 bytes of ECC apply on Read Long/Write Long commands

55H Disable read look-ahead feature

66H Disable reverting to power on defaults

82H Disable write cache

85H Disable Advanced Power Management (See note 3)

89H Disable Address Offset mode

AAH Enable read look-ahead feature

BBH 4 bytes of ECC apply on Read Long/Write Long commands

CCH Enable reverting to power on defaults

Note 1. When the Feature register is 03h (= Set Transfer mode) the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

```
PIO Default Transfer Mode                      00000 000
PIO Default Transfer Mode,Disable IORDY        00000 001
PIO Flow Control Transfer Mode x 00001 nnn     (nnn=000,001,010,011,100)
Multiword DMA mode x 00100 nnn                 (nnn=000,001,010)
Ultra DMA mode x 01000 nnn                     (nnn=000,001,010,011,100)
```

When the Feature register is 05h (= Enable Advanced Power Management) the Sector Count Register specifies the Advanced Power Management level.

```
C0h–FEh        The deepest Power Saving mode is Active Idle
80h–BFh        The deepest Power Saving mode is Low power Idle
01h–7Fh        The deepest Power Saving mode is Standby
00h, FFh       Aborted
```

Note 2. If the number of auto reassigned sectors reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command (with Feature register = 02h) without error, the write cache function will remain disabled. For the current write cache function status, refer to the Identify Device Information (129 word) by the Identify Device command.

Hard reset or power off must not be done in 5 seconds after write command completion when write cache is enabled.

Note 3. When the Feature register is 85h (= Disable Advanced Power Management) the deepest Power Saving mode becomes Active Idle.

13.29 Set Max ADDRESS (F9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	V V V V V V V V		Error	see below
Sector Count	– – – – – – – B		Sector Count	– – – – – – – –
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	– – – – H H H H
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 106. Set Max ADDRESS (F9h)

The Set Max ADDRESS command overwrites the max LBA/CYL of HDD in a range of actual device capacities. Once the device receives this command, all accesses beyond that LBA/CYL are rejected by setting the ABORT bit in the status register. Identify the device command and Identify the device DMA command returns the LBA/CYL which is set via this command as a default value.

This command implement SET MAX security extension commands as subcommands. But regardless of Feature register value, the case this command is immediately preceded by a Read Native Max ADDRESS command, it is interpreted as a Set Max ADDRESS command.

The Read Native Max ADDRESS command should be issued and completed immediately prior to issuing the Set Max ADDRESS command. If it is not, this command is interpreted as a Set Max security extension command which is designated by feature register.

If Set Max security mode is in the Locked or Frozen, the Set Max ADDRESS command is aborted.

For more information, see section 11.9.2, “Set Max security extension commands” on page 89.

In CHS mode, Cylinder High, Cylinder Low specify the maximum cylinder number. The Head number of DEVICE/HEAD and Sector Number are ignored. The default value (see default CHS in Identify device information) is used for that.

In LBA mode, the Head number of DEVICE/HEAD , the Cylinder High, the Cylinder Low, and the Sector Number specify the max LBA. This command will set this LBA as the max LBA of the device.

Output Parameters To The Device

Feature Destination code for this command

00h na
01h SET MAX SET PASSWORD
02h SET MAX LOCK
03h SET MAX UNLOCK
04h SET MAX FREEZE LOCK

When the Set Max ADDRESS command is executed, this register is ignored.

B This indicates the option bit for selection whether nonvolatile or volatile. B = 0 is the volatile condition. When B = 1, MAX LBA/CYL—which is set by the Set Max ADDRESS command—is preserved by POR and HARD RESET. When B = 0, MAX LBA/CYL—which is set by Set Max ADDRESS command—will be lost by POR and HARD RESET. B = 1 is not valid when the device is in Address Offset mode and the command is aborted.

Sector Number In LBA mode this register contains LBA bits 0–7 which are to be input. (L = 1) In CHS mode this register is ignored. (L = 0)

Cylinder High/Low In LBA mode this register contains LBA bits 8–15 (Low) and bits 16–23 (High) which are to be set. (L = 1)

In CHS mode this register contains the cylinder number which is to be input. (L = 0)

H In LBA mode this register contains LBA bits 24–27 which are to be input. (L = 1)

In CHS mode this register is ignored. (L = 0)

L This indicates the LBA addressing mode. L = 0 specifies the CHS mode and L = 1 specifies the LBA addressing mode.

D This indicates the device number bit. The device number bit of the Device/Head should be specified. D = 0 selects the master device and D = 1 selects the slave device.

V This indicates Valid. The bit is part of an output parameter and should be specified.

- This indicates that the bit is not used.

Input Parameters From The Device

Sector Number In LBA mode this register contains the Adjusted max. LBA bits 0–7.(L = 1)

In CHS mode this register contains the maximum sector number (= 63). (L = 0)

Cylinder High/Low In LBA mode this register contains the Adjusted max. LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

In CHS mode this register contains the max. cylinder number which is set. (L = 0)

H In LBA mode this register contains the Adjusted max. LBA bits 24–27. (L = 1)

In CHS mode this register contains the maximum head number (= 15). (L = 0)

V Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.

- This indicates that the bit is not used.

13.30 Set Multiple (C6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – H H H H
Command	1 1 0 0 0 1 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 107. Set Multiple command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up or hard reset is 0. The Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host. The Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count. This indicates the block size to be used for the Read Multiple and the Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then the Read Multiple and the Write Multiple commands are disabled.

13.31 Sleep (E6h/99h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 1 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 108. Sleep command (E6h/99h)

This command is the only way to cause the device to enter Sleep Mode.

When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down, and the interface becomes inactive. The only way to recover from Sleep Mode is with a software reset or a hardware reset.

The use of hardware reset to recover from Sleep Mode may be incompatible with continued operation of the host system.

If the device is already spun down, the spin down sequence is not executed.

13.32 S.M.A.R.T. Function Set (B0h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	V V V V V V V V		Error	see below
Sector Count	V V V V V V V V		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	0 1 0 0 1 1 1 1		Cylinder Low	– – – – – – – –
Cylinder High	1 1 0 0 0 0 1 0		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 0 1 1 0 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 109. S.M.A.R.T. Function Set command (B0h)

The S.M.A.R.T. Function Set command provides access to the Attribute Values, the Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which are selectable via the device's Features Register when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Code Subcommand

D0h S.M.A.R.T. Read Attribute Values

D1h S.M.A.R.T. Read Attribute Thresholds

D2h S.M.A.R.T. Enable/disable Attribute Autosave

D3h S.M.A.R.T. Save Attribute Values

D4h S.M.A.R.T. Execute Off-line Immediate

D5h S.M.A.R.T. Read Log Sector

D6h S.M.A.R.T. Write Log Sector

D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
Dah	S.M.A.R.T. Return Status
Dbh	S.M.A.R.T. Enable/Disable Automatic Off-line

13.32.1 S.M.A.R.T. Function Subcommands

13.32.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the S.M.A.R.T. Read Attribute Values subcommand from the host, the device asserts BSY, saves any updated Attribute Values to the Attribute Data sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

13.32.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the S.M.A.R.T. Read Attribute Thresholds subcommand from the host, the device asserts BSY, reads the Attribute Thresholds from the Attribute Threshold sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device via the Data Register.

13.32.1.3 S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h)

This subcommand enables and disables the attribute auto save feature of the device. The S.M.A.R.T. Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector at the timing of the first transition to Active idle mode and after 30 minutes after the last saving of Attribute Values. This subcommand causes the auto save feature to be disabled. The state of the Attribute Autosave feature—either enabled or disabled—will be preserved by the device across the power cycle.

A value of 00h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or a power-down.

A value of F1h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will not change the current Autosave status. The device will respond with the error code specified in Figure 120 on page 175.

The S.M.A.R.T. Disable Operations subcommand disables the auto save feature along with the device's S.M.A.R.T. operations.

Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY, and asserts INTRQ.

13.32.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the S.M.A.R.T. Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY, and asserts INTRQ.

13.32.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The Sector Number register shall be set to specify the operation to be executed.

Sector Number	Operation to be executed
0	Execute S.M.A.R.T. off-line data collection routine immediately
1	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
2	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
127	Abort off-line mode self-test routine
129	Execute S.M.A.R.T. Short self-test routine immediately in captive mode
130	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (Figure 110 on page 164) and ATA registers—see definitions below—and then executes the command completion.

Status	Set ERR to one when the self-test has failed
Error	Set ABRT to one when the sellf-test has failed
Cyl Low	Set to F4h when the self-test has failed
Cyl High	Set to 2Ch when the self-test has failed

13.32.1.6 S.M.A.R.T. Read Log Sector (subcommand D5h)

This command returns the specified log sector contents to the host.

The 512 bytes of data are returned at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address.

Log sector address	Content	Type
01h	S.M.A.R.T. Error Log	Read Only
06h	S.M.A.R.T. Self-test Log	Read Only
80h–9Fh	Host vendor specific	Read/Write

Figure 110. Log sector addresses

13.32.1.7 S.M.A.R.T. Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector.

The 512 bytes of data are transferred at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address (Figure 109). If a Read Only log sector is specified, the device returns ABRT error.

13.32.1.8 S.M.A.R.T. Enable Operations (subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a S.M.A.R.T. Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T.—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent S.M.A.R.T. Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the S.M.A.R.T. Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

13.32.1.9 S.M.A.R.T. Disable Operations (subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the device's attribute auto save feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T.—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.

Upon receipt of the S.M.A.R.T. Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of the device of the S.M.A.R.T. Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands—with the exception of S.M.A.R.T. Enable Operations—are disabled, and invalid and will be aborted by the device—including the S.M.A.R.T. Disable Operations subcommand—returning the error code as specified in Figure 120 on page 175.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the S.M.A.R.T. Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a S.M.A.R.T. Read Attribute Values or a S.M.A.R.T. Save Attribute Values command.

13.32.1.10 S.M.A.R.T. Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the S.M.A.R.T. Return Status subcommand the device asserts BSY, saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, or detects a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register, clears BSY, and asserts INTRQ.

If the device detects a Threshold Exceeded Condition for prefailure attributes, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register, clears BSY, and asserts INTRQ. Advisory attributes never result in a negative reliability condition.

13.32.1.11 S.M.A.R.T. Enable/Disable Automatic Off-Line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities.

The Sector Count register shall be set to specify the feature to be enabled or disabled.
Enable Off-line Read Scanning F9h
Enable Automatic Off-line F8h
Disable Off-line Read Scanning 01h
Disable Automatic Off-line 00h
Feature Description Sector Count

A value of zero—written by the host into the device's Sector Count register before issuing this subcommand—shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation—such as during a power-on, during a power-off sequence, or during an error recovery sequence.

A value of one written by the host into the device's Sector Count register before issuing this subcommand shall cause the off-line read scanning feature to be disabled. The Device does not perform the off-line read scanning at the off-line data collection activities which is initiated by the S.M.A.R.T. Execute Off-line Immediate(Subcommand D4h) or automatically if the off-line read scanning feature is disabled.

A value of F8h—written by the host into the device's Sector Count register before issuing this subcommand—shall cause the automatic Off-line data collection feature to be enabled.

A value of F9 written by the host into the device's Sector Count register before issuing this subcommand shall cause the off-line read scanning feature to be enabled. The Device perform the off-line read scanning at the off-line data collection activities which is initiated by the S.M.A.R.T. Execute Off-line Immediate(Subcommand D4h) even if the automatic off-line feature is disabled.

Any other non-zero value—written by the host into this register before issuing this subcommand—is vender specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in Figure 120 on page 175.

13.32.2 Device Attributes Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Values subcommand. All multibyte fields shown in these data structures follow the ATA/ATAPI-5 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

Description	Byte	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0010h
1st Device Attribute	12	02h	(*1)	(*2)
2nd Device Attribute	12	0Eh	(*1)	(*2)
3nd Device Attribute	12	1Ah	(*1)	(*2)
↕	↕	↕	↕	↕
30th Device Attribute	12	15Eh	(*1)	(*2)
Off–line data collection status	1	16Ah	(*1)	(*2)
Self–test execution status	1	16Bh	(*1)	(*2)
Total time in seconds to complete off–line data collection activity	2	16Ch	(*1)	(*2)
Current segment pointer	1	16Eh	(*1)	(*2)
Off–line data collection capability	1	16Fh	(*1)	1Bh
S.M.A.R.T. capability	2	170h	(*1)	0003h
S.M.A.R.T. device error logging capability	1	172h	(*1)	01h
Self–test failure check point	1	173h	(*1)	(*2)
Short self–test completion time in minutes	1	174h	(*1)	(*2)
Extended self–test completion time in minutes	1	175h	(*1)	(*2)
Reserved	12	176h		00h
Vendor specific	125	182h		00h
Data structure checksum	1	1FFh	(*1)	(*2)
	512			

(*1) – See paragraphs 13.32.2.1, 13.32.2.12, 13.32.2.2, 13.32.2.2, and13.32.2.2 for definitions of titles in the Description column.
(*2) – This value varied due to actual operating condition.

Figure 111. Device Attribute Data Structure

13.32.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

13.32.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Description	Byte	Offset	Value
Attribute ID Number (01h to FFh)	1	00h	binary
Status Flags	2	01h	bit flags
Bit 0 Pre–Failure/Advisory			
Bit 1 On–line Collection			
Bit 2–5 Reserved (may either 0			
Bit 6–15 Reserved (all 0)			
Attribute Value (valid values from 01h to FEh)	1	03h	binary
00h invalid for attribute value – not to be used			
01h minimum value			
64h initial value for all attributes prior to any data collection			
FDh maximum value			
FEh value is not valid			
FFh invalid for attribute value – not to be used			
Reserved (may not be 0)	1	04h	binary
Reserved (may not be 0)	6	05h	binary
Reserved (00h)	1	0Bh	binary
Total Bytes	12		

Figure 112. Individual Attribute Data Structure

Attribute ID Numbers: Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers. The names marked with (*) indicate that the corresponding Attribute Values can be either collected on-line or off-line.

ID Attribute Name

0 Indicates that this entry in the data structure is not used

1 Raw Read Error Rate (*)

2 Throughput Performance (*)

3 Spin Up Time

4 Start/Stop Count

5 Reallocated Sector Count

7 Seek Error Rate

8 Seek Time Performance (*)

9 Power-On Hours Count

10 Spin Retry Count

12 Device Power Cycle Count

191 Gsense Error Rate

192 Power Off Retract Count

193 Load/Unload Cycle Count

196 Reallocation Event Count

197 Current Pending Sector Count

198 Off-Line Scan Uncorrectable Sector Count

199 Ultra DMA CRC Error Count

Status Flag definitions:

Bit	Flag Name	Definition
0	Pre–Failure/ Advisory bit	If bit = 0, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates an Advisory condition where the usage or age of the device has exceeded its intended design life period. If bit = 1, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates a Pre–Failure condition where imminent loss of data is being predicted.
1	On–Line Collective bit	If bit = 0, the Attribute Value is updated only during Off–Line testing. If bit = 1, the Attribute Value is updated during On–Line testing or during both On–Line and Off–Line testing.
2–5	Reserved bits	may either 0 or 1
6–15	Reserved bits	Always 0

Figure 113. Status Flag definitions

Normalized values: The device will perform conversion of the raw Attribute Values to transform them into normalized values which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value. In normalizing the raw data, the device will perform any necessary statistical validity checks to ensure that an instantaneous raw value is not improperly reflected in the normalized Attribute Value (i.e., one read error in the first 10 reads being interpreted as exceeding the read error rate threshold when the subsequent 1 billion reads all execute without error). The end points for the normalized values for all Attributes will be 1 (01h) at the low end, and 100 (64h) at the high end for the device. For Performance and Error Rate Attributes, values greater than 100 are also possible. The maximum value possible is 253 (FDh).

13.32.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates an Automatic Off-line Data Collection Status.

Bit 7 Automatic Off-line Data Collection Status

0 Automatic Off-line Data Collection is disabled.

1 Automatic Off-line Data Collection is enabled.

Bits 0–6 represents a hexadecimal status value reported by the device.

Value Definition

0 Off-line data collection never started.

2 All segments completed without errors. In this case the current segment pointer is equal to the total segments required.

4 Off-line data collection is suspended by the interrupting command.

5 Off-line data collecting is aborted by interrupting command.

6 Off-line data collection is aborted with a fatal error.

13.32.2.4 Self-test execution status

Bit Definition

0-3 Percent Self-test remaining.

An approximation of the percent of the self-test routine remaining until completion given in ten percent increments. Valid values are 0 through 9.

4-7 Current Self-test execution status.

0 The self-test routine completed without error or has never been run.

1 The self-test routine was aborted by the host.

2 The self-test routine was interrupted by the host with a hard or soft reset.

3 The device was unable to complete the self-test routine due to a fatal error or unknown test error.

4 The self-test routine was completed with an unknown element failure.

5 The self-test routine was completed with an electrical element failure.

6 The self-test routine was completed with a servo element failure.

7 The self-test routine was completed with a read element failure.

15 The self-test routine is in progress.

13.32.2.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

13.32.2.6 Current segment pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. Because the number of segments is 1, 01h is always returned in this field.

13.32.2.7 Off-line data collection capability

Bit Definition

0 The Execute Off-line Immediate implemented bit

0 S.M.A.R.T. Execute Off-line Immediate subcommand is not implemented

1 S.M.A.R.T. Execute Off-line Immediate subcommand is implemented

1 Enable/disable Automatic Off-line implemented bit

0 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is not implemented

1 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is implemented

2 Abort/restart off-line by host bit

0 The device will suspend off-line data collection activity after an interrupting command and resume it after some vendor specific event

1 The device will abort off-line data collection activity upon receipt of a new command

3 Off-line Read Scanning implemented bit

0 The device does not support Off-line Read Scanning

1 The device supports Off-line Read Scanning

4 Self-test implemented bit

0 Self-test routing is not implemented

1 Self-test routine is implemented

5-7 Reserved (0)

13.32.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit Definition

0 Pre-power mode attribute saving capability

If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).

1 Attribute auto save capability

If bit = 1, the device supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

2-15 Reserved (0)

13.32.2.9 Error logging capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit If bit = 1, the device supports the Error Logging

13.32.2.10 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

13.32.2.11 Self-test completion time

These bytes are the minimum time in minutes to complete the self-test.

13.32.2.12 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

13.32.3 Device Attribute Thresholds data structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multibyte fields shown in these data structures follow the ATA/ATAPI-5 specification for byte ordering. This means that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Description	Byte	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0010h
1st Device Attribute	12	02h	(*1)	(*2)
...	..			
...	..			
30th Device Attribute	12	15Eh	(*1)	(*2)
Reserved	18	16Ah		00h
Vendor specific	131	17Ch		00h
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See the following definitions
(*2) – Value varied by actual operating condition

Figure 114. Device Attribute Thresholds Data Structure

13.32.3.1 Data Structure revision number

This value is the same as the value used in the Device Attributes Values Data Structure.

13.32.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Description	Byte	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary

Attribute Threshold (for comparison with Attribute Values from 00h to FFh)	1	01h	binary
00h – "always passing" threshold value to be used for code test purposes			
01h – minimum value for normal operation			
FDh – maximum value for normal operation			
FEh – invalid for threshold value			
FFh – "always failing" threshold value to be used for code test purposes			
Reserved (00h)	10	02h	binary
Total Bytes	12		

Figure 115. Individual Threshold Data Structure

13.32.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

13.32.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable. However, the host might use the "S.M.A.R.T. Write Attribute Threshold" subcommand to override these preset values in the Threshold sectors.

13.32.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

13.32.4 S.M.A.R.T. error log sector

The following defines the 512 bytes that make up the S.M.A.R.T. error log sector. All multibyte fields shown in these data structures follow the ATA/ATAPI-5 specifications for byte ordering.

Description	Byte	Offset
S.M.A.R.T. error log version	1	00h
Error log pointer	1	01h
1st error log data structure	90	02h
2nd error log data structure	90	5Ch
3rd error log data structure	90	B6h
4th error log data structure	90	110h
5th error log data structure	90	16Ah
Device error count	2	1C4h
Reserved	57	1C6h
Data structure checksum	1	1FFh
	512	

Figure 116. S.M.A.R.T. error log sector

13.32.4.1 S.M.A.R.T. error log version

This value is set to 01h.

13.32.4.2 Error log pointer

This points to the most recent error log data structure. Only values 1 through 5 are valid.

13.32.4.3 Device error count

This field contains the total number of errors. The value will not roll over.

13.32.4.4 Error log data structure

The data format of each error log structure is shown below.

Description	Byte	Offset
1st command data structure	12	00h
2nd command data structure	12	0Ch
3rd command data structure	12	18h
4th command data structure	12	24h
5th command data structure	12	30h
Error data structure	30	3Ch
	90	

Figure 117. Error log data structure

Command data structure: Data format of each command data structure is shown below.

Description	Byte	Offset
Device Control register	1	00h
Features register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Command register	1	07h
Time stamp (milliseconds from Power On)	4	08h
	12	

Figure 118. Command data structure

13.32.4.4.1 Error data structure

Data format of error data structure is shown below.

Description	Byte	Offset
Reserved	1	00h
Error register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Status register	1	07h
Extended error data (vendor specific)	19	08h
State	1	1Bh
Life time stamp (hours)	2	1Ch
	30	

Figure 119. Error data structure

State field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	S.M.A.R.T. Off-line or Self-test
x5h–xAh	Reserved
xBh–xFh	Vendor specific

Note: The value of the x is vendor specific.

13.32.5 Self-test log data structure

The following defines the 512 bytes that make up the Self-test log sector. All multibyte fields shown in these data structures follow the ATA/ATAPI-5 specifications for byte ordering.

Description	Byte	Offset
Data structure revision	2	00h
Self-test number	1	n*18h+02h
Self-test execution status	1	n*18h+03h
Life time power on hours	2	n*18h+04h
Self-test failure check point	1	n*18h+06h
LBA of first failure	4	n*18h+07h
Vendor specific	15	n*18h+08h
...		
Vendor specific	2	1FAh
Self-test log pointer	1	1FCh
Reserved	2	1FDh
Data structure checksum	1	1FFh
	512	

Figure 120. Self-test log data structure

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors.

After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor.

The self-test log pointer points to the most recent descriptor. When there is no descriptor the value is 0. When there are descriptor(s) the value is 1 through 21.

13.32.6 Error reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Error condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. Disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure.	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h or 01h

Figure 121. S.M.A.R.T. Error Codes

13.33 Standby (E2h/96h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	V V V V V V V V		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 0 1 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 122. Standby command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately and to set the auto power down time-out parameter (standby timer).

When this command is issued, the device confirms the completion of the cached write commands before it asserts the INTRQ. Following the INTRQ the interface remains active and the device is spun down.

If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, however there will be a delay while waiting for the spindle to reach operating speed.

The timer starts counting down when the device returns to Idle mode.

Output Parameters To The Device

Sector Count The Time-out Parameter. If it is zero the time-out interval (Standby Timer) is NOT disabled but is automatically set to 109 minutes. If it is other than zero the time-out interval is set for (Time-out Parameter × 5) seconds.

When the automatic power down sequence is enabled, the device will enter the Standby mode automatically if the time-out interval expires with no device access from the host. The time-out interval will be reinitialized if there is a device access before the time-out interval expires.

13.34 Standby Immediate (E0h/94h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 0 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	–	0	–	V

Figure 123. Standby Immediate command (E0h/94h)

The Standby Immediate command causes the device to enter the Standby mode immediately.

When this command is issued, the device confirms the completion of the cached write commands before it asserts the INTRQ. Following the INTRQ the interface remains active and the device is spun down.

If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, however there will be a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down time-out parameter.

13.35 Write Buffer (E8h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –		Data	– – – – – – – –
Feature	– – – – – – – –		Error	see below
Sector Count	– – – – – – – –		Sector Count	– – – – – – – –
Sector Number	– – – – – – – –		Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –		Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –		Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –		Device/Head	– – – – – – – –
Command	1 1 1 0 1 0 0 0		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	–	–	0	–	V

Figure 124. Write Buffer command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

13.36 Write DMA (CAh/CBh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 1 0 1 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 125. Write DMA command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device and then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This indicates the retry bit. If the retry bit is set to one then retries are disabled. When the write cache is enabled the retry bit is ignored. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.37 Write Long (32h/33h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 1 0 0 1 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 126. Write Long command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are either 4 or 40 according to setting of the Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R The retry bit. If the retry bit is set to one, then retries are disabled.

Input Parameters From The Device

Sector Count This indicates the number of requested sectors not transferred.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode this register contains current the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode this register contains current the LBA bits 24–27. (L = 1)

The file internally uses 40 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 40 byte ECC mode is used for all tests to confirm the operation of the files ECC hardware. Unexpected results may occur if such testing is performed using 4 byte mode.

13.38 Write Multiple (C5h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 0 1 0 1		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 127. Write Multiple command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, then the data is written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block—as defined by the Set Multiple command—instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. If the Sector Count of zero is specified, then 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

Input Parameters From The Device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero, unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains current the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the last transferred sector. (L = 0)

In LBA mode this register contains current the LBA bits 24–27. (L = 1)

13.39 Write Sectors (30h/31h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 1 0 0 0 R		Status	see below

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 128. Write Sectors command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device. The data is then written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector, when the auto reassign function is disable.

Output Parameters To The Device

Sector Count This indicates the number of continuous sectors to be transferred. If the Sector Count of zero is specified, then 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This indicates the retry bit. If the retry bit is set to one then retries are disabled. When the write cache is enabled the retry bit is ignored. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.40 Write Verify (3Ch: vendor specific)

In DJSA-XXX implementation, the Write Verify command is exactly the same as Write Sectors command (30h). No read verification is performed after the write operation.

Refer to 13.39, “Write Sectors Command,” on page 185 for parameters.

14.0 Time-out values

The timing of BSY and DRQ in Status Register are shown in the table below.

	INTERVAL	START	STOP	TIME-OUT
Power On	Device Busy After Power On	Power On	Status Register BSY=1	400 ns
	Device Ready After Power On	Power On	Status Register BSY=1 and RDY=1	31 sec
Software Reset	Device Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Device Ready After Software Reset	Device Control Register RST=0 After RST=1	Status Register BSY=0 and RDY=1	31 sec
Hard Reset	Device Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Device Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Device Busy After Command Code Out	OUT To Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	30 sec
	Device Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	700 us *(Note 3.)*
	Device Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and RDY=1 Interrupt	30 sec *(Note 1.)*
Non-Data Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	30 sec *(Note 2.)*
DMA Data Transfer Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns

Figure 129. Time-out values

Command category is referred to in section 12.0, "Command protocol" on page 97.

We recommend that the host system executes Soft reset and then retry to issue the command if the host system time-out would occur for the device.

(Note 1.) For SECURITY ERASE UNIT command, the execution time is referred to 13.22, "Security Erase Unit (F4h)" on page 143.

(Note 2.) For FORMAT UNIT command, the execution time is referred to 13.6, "Format Unit (F7h: Vendor Specific)" on page 113.

(Note 3.) When the initial power mode at power on is Standby mode, and when the following commands are issued by the host as First Command, the command's time-out value of the field is 10 seconds.

Security Disable Password, Security Erase Unit,

Security Set Password, Security Unlock.

15.0 Appendix

15.1 Commands Support Coverage

Following table is provided to facilitate the understanding of DJSA-XXX command support coverage comparing to the ATA-5 defined command set. The column of 'Implementation' shows the capability of DJSA-XXX for those commands.

Command Code	Command Name	Implementation for DJSA-XXX	ATA-5 Category Type
00h	NOP	No	Optional
03h	CFA REQUEST EXTENDED ERROR CODE	No	Optional (7)
08h	DEVICE RESET	No	Optional (7)
1xh	RECALIBRATE	Yes	obsoleted
20h	READ SECTOR(S) (w/ retry)	Yes	Mandatory
21h	READ SECTOR(S) (w/o retry)	Yes	obsoleted
22h	READ SECTOR(S) (w/ retry)	Yes	obsoleted
23h	READ LONG (w/o retry)	Yes	obsoleted
30h	WRITE SECTOR(S) (w/ retry)	Yes	Mandatory
31h	WRITE SECTOR(S) (w/o retry)	Yes	obsoleted
32h	WRITE LONG (w/ retry)	Yes	obsoleted
33h	WRITE LONG (w/o retry)	Yes	obsoleted
38h	CFA TRANSLATE SECTORS W/O ERASE	No	Optional (7)
3Ch	WRITE VERIFY (2)	Vendor specific	obsoleted
40h	READ VERIFY SECTOR (S) (w/retry)	Yes	Mandatory
41h	READ VERIFY SECTORS (S) (w/o retry)	Yes	obsoleted
50h	FORMAT TRACK	Yes	obsoleted
7xh	SEEK	Yes	Mandatory
87h	CFA TRANSLATE SECTORS	No	Optional
90h	EXECUTE DEVICE DIAGNOSTIC	Yes	Mandatory
91h	INITIALIZE DEVICE PARAMETERS	Yes	Mandatory
92h	DOWNLOAD MICROCODE	Reserved	Optional
94h–99h	Reserved	Reserved	Reserved
A0h	PACKET	No	Not to be used
A1h	IDENTIFY PACKET DEVICE	No	Not to be used
A2H	SERVICE	No	Not to be used
B0h	S.M.A.R.T. FUNCTION SET	Yes	Optional – (5)
C0h	CFA ERASE SECTORS	No	Optional
C4h	READ MULTIPLE	Yes	Mandatory
C5h	WRITE MULTIPLE	Yes	Mandatory
C6h	SET MULTIPLE MODE	Yes	Mandatory
C7h	READ DMA QUEUED	No	Optional
C8h	READ DMA (w/ retry)	Yes	Mandatory
C9h	READ DMA (w/o retry)	Yes	obsoleted

Figure 130. Command coverage (1 of 2)

Command Code	Command Name	Implementation for DJSA-XXX	ATA-5 Command Type
CAh	WRITE DMA (w/ retry)	Yes	Mandatory
CBh	WRITE DMA (w/o retry)	Yes	obsoleted
CCh	WRITE DMA QUEUED	No	Optional
CDh	CFA WRITE MULTIPLE W/O ERASE	No	Optional – (7)
DAh	GET MEDIA STATUS	No	Optional (7)
DEh	MEDIA LOCK	No	Optional (7)
DFh	MEDIA UNLOCK	No	Optional (7)
E0h	STANDBY IMMEDIATE	Yes	Mandatory
E1h	IDLE IMMEDIATE	Yes	Mandatory
E2h	STANDBY	Yes	Mandatory
E3h	IDLE	Yes	Mandatory
E4h	READ BUFFER	Yes	Optional
E5h	CHECK POWER MODE	Yes	Mandatory
E6h	SLEEP	Yes	Mandatory
E7h	FLUSH CACHE	Yes	Mandatory
E8h	WRITE BUFFER	Yes	Optional
ECh	IDENTIFY DEVICE	Yes	Mandatory
EDh	MEDIA EJECT	No	Optional (7)
EEh	IDENTIFY DEVICE DMA	Yes	obsoleted
EFh	SET FEATURES	Yes	Mandatory
F0h	SENSE CONDITION	Vendor specific	Vendor specific
F1h	SECURITY SET PASSWORD	Yes	Optional (6)
F2h	SECURITY UNLOCK	Yes	Optional (6)
F3h	SECURITY ERASE PREPARE	Yes	Optional (6)
F4h	SECURITY ERASE UNIT	Yes	Optional (6)
F5h	SECURITY FREEZE LOCK	Yes	Optional (6)
F6h	SECURITY DISABLE PASSWORD	Yes	Optional (6)
F7h	FORMAT UNIT	Vendor specific	Vendor specific
F8h	READ NATIVE MAX ADDRESS	Yes	Optional
F9h	SET MAX ADDRESS	Yes	Optional
FAh	ENABLE/DISABLE DELAYED WRITE	Yes	Vendor specific
FBh	Vendor specific	Reserved	Vendor specific
	Reserved: all remaining codes	Reserved	Reserved

Note:

(1) *These commands have two command codes and appear in this table twice, once for each command code.*

(2) *The WRITE VERIFY command implemented vendor specific. The operation is same as WRITE SECTORS and verification is not performed.*

(3) *Protected Area Feature Set*

(4) *Power Management Feature Set*

(5) *S.M.A.R.T. Function Set*

(6) *Security Mode Feature Set*

(7) *Removable*

Figure 130. Command coverage (2 of 2)

15.2 SET FEATURES Command Support Coverage

The following table provides a list of Feature Registers, Feature Names, and implementation for the DJSA-XXX models. The "Implementation" column indicates with a "Yes" or "No" whether or not the DJSA-XXX models have the capability of executing the command in comparison to the ATA/ATAPI-5 defined command set. For detail operation, refer to section 13.28, "Set Features (EFh)" on page 153.

Features Register	Features Name	Implementation for DJSA-XXX
02h	Enable write cache	Yes
03h	Set transfer mode	Yes
05h	Enable Advanced Power Management	Yes
09h	Enable Address Offset mode	Yes
44h	Set vendor specific bytes ECC	Yes
55h	Disable read look–ahead feature	Yes
5Dh	Enable release interrupt	No
5Eh	Enable SERVICE interrupt	No
66h	Disable reverting to power on defaults	Yes
82h	Disable write cache	Yes
85h	Disable Advanced Power Management	Yes
89h	Disable Address Offset mode	Yes
95h	Enable Media Status Notification	No
AAh	Enable read look–ahead feature	Yes
BBh	Set 4 bytes ECC	Yes
CCh	Enable reverting to power on defaults	Yes
DDh	Disable release interrupt	No
EEh	Disable SERVICE interrupt	No
others	Reserved	Reserved

Figure 131. SET FEATURES command coverage

15.3 Changed Points from DARA-XXXXXX

DJSA-XXX specification changed some features contained in the DARA-XXXXXX specification.

The changed points are listed below.

- The identify device information data changed.
- The Condition Sense command is implemented in the DJSA-XXX specification.

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